S6B0729

102 SEG / 81 COM DRIVER & CONTROLLER FOR 4 GRAY SCALE STN LCD

Jun.19. 2001.

Ver. 0.1

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

S6B0729 Specification Revision History		
Version	**Content**	**Date**
0.0	Preliminary specification (short form)	June 8, 2001
0.1	Preliminary specification (full set)	June 19, 2001

CONTENTS

INTRODUCTION

The S6B0729 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 102 segment and 81 common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit parallel display data and stores in an on-chip display data RAM of 102 x 81 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM and FRC Methods

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Dark

(Accessible column address, n = 0, 1, 2, ….., 99, 100, 101)

Driver Output Circuits

– 102 segment outputs / 81 common outputs

Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/16 ~ 1/80 (ICON disabled) 1/17 ~ 1/81 (ICON enabled)	1/4 to 1/10	81 × 102

– Various partial display
– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 81 × 102 × 2 = 16,524bits

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– SPI (serial peripheral interface) available (only write operation)

On-chip Low Power Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x3, x4, ×5)
– Voltage regulator (temperature coefficient: -0.125%/°C, or external input)
– On-chip electronic contrast control function (64 steps)
– Voltage follower (LCD bias :1/4 to 1/10)

Operating Voltage Range

– Supply voltage (V_{DD}): 1.8 to 3.3V
– Converter input voltage(Vci): 2.4 to 3.3 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 11.0 V

Low Power Consumption

- 60 μA Typ. (operation) : Vdd=Vci=2.5V, VLCD=9.004V, x5 boosting, No load
- 2 μA Max. (sleep mode)

Package Type

- Gold bumped chip or TCP

BLOCK DIAGRAM

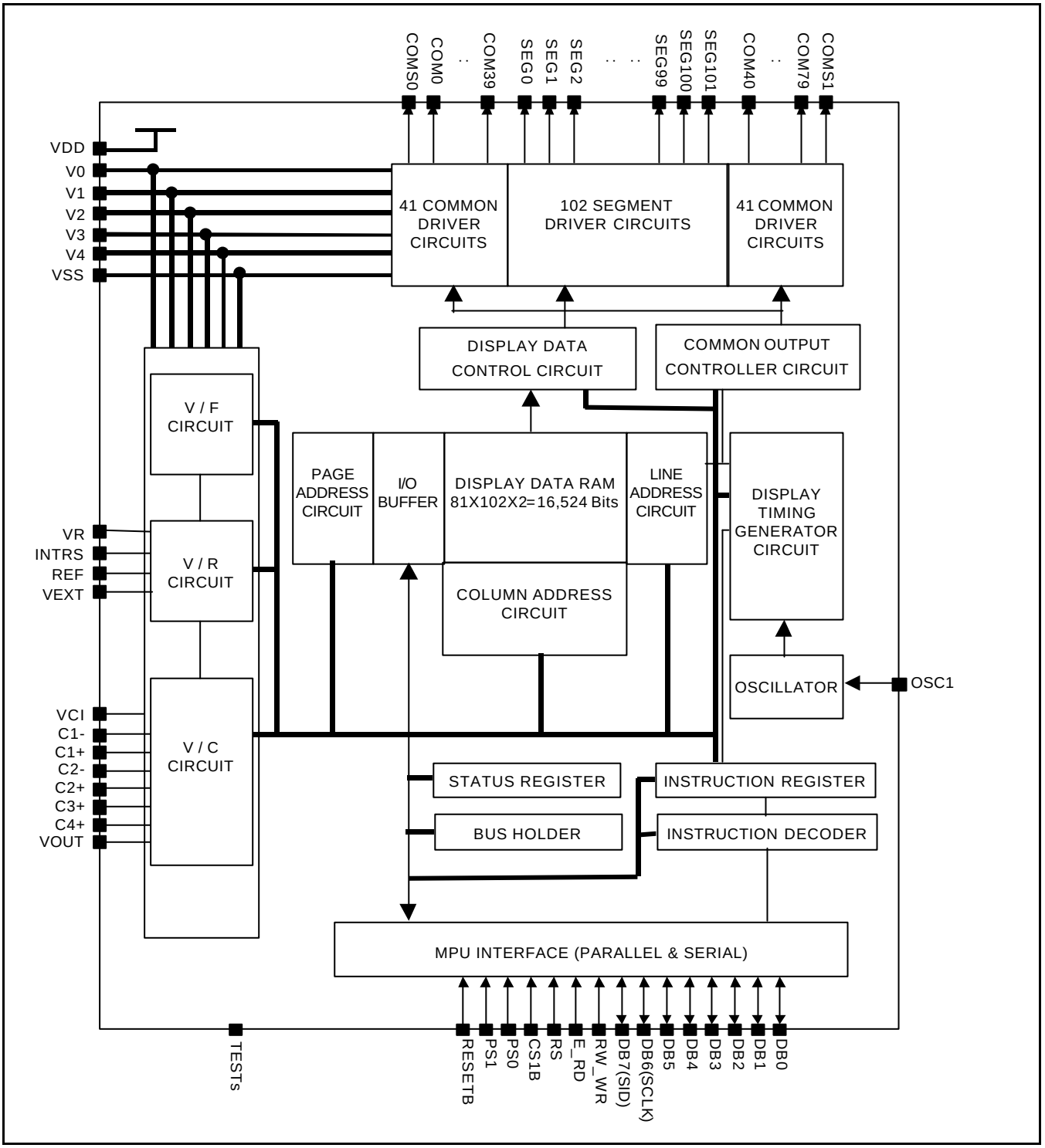


Figure 1. Block Diagram

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
<tr><td colspan="5">NOTE: N = 4,5,9,10</td></tr>
</table>
</td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
V0	I/O	LCD Power supply input / output pin Connect this pin to VSS through capacitor
VOUT	I/O	Voltage converter input / output pin Connect this pin to VSS through capacitor
VCI	I	Voltage converter input voltage pin
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L") When using internal resistors (INTRS = "H"), open this pin
REF	I	Selects the external VREF voltage via the VEXT pin – REF = " H" : using the internal VREF – REF = " L" : using the external VREF
VEXT	I	Externally input reference voltage (VREF) for the internal voltage regulator It is valid only when REF is "L" When using internal voltage regulator, connect to VDD, VSS or open this pin

OSC1	I	When using internal clock oscillator, connect a resistor between OSC1 and VDD.

SYSTEM CONTROL

Table 5. System Control Pin Description

Name	I/O	Description
INTRS	I	Internal resistor select pin This pin selects the resistors for adjusting V0 voltage level – INTRS = "H": use the internal resistors. – INTRS = "L": use the external resistors VR pin and external resistive divider control V0 voltage
TESTs	O	Test pins Don' t use this pin. – TESTs: Open this pin.

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="5">PS0</td><td rowspan="5">I</td><td>Parallel / Serial data input select input</td></tr>
<tr><td>
<table>
<tr><td>PS0</td><td>Interface mode</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>RS or None</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table>
</td></tr>
<tr><td>*NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>PS1</td><td>I</td><td>Microprocessor interface select input pin
– PS0 = “H”, PS1 = "H": 6800-series parallel MPU interface
– PS0 = “H”, PS1 = "L": 8080-series parallel MPU interface
– PS0 = “L”, PS1 = "H": 4 pin-SPI MPU interface
– PS0 = “L”, PS1 = "L": 3 pin-SPI MPU interface</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is "L". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="3">RW_WR</td><td rowspan="3">I</td><td>Read / Write execution control pin</td></tr>
<tr><td>
<table>
<tr><td>C68</td><td>MPU type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = “H” : read
– RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
</table>

Table 7. Microprocessor Interface Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>PS1</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS0 = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 8. LCD Driver Output Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG101</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM79</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M (Internal)</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">VSS</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS
(COMS1)</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

NOTE: **DUMMY – These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The S6B0729 can interface with an MPU when CSB is "L". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B0729 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 9.

Table 9. Parallel / Serial Interface Mode

Type	PS1	CSB	PS0	Interface mode
Parallel	H	CSB	H	6800-series MPU mode
	L			8080-series MPU mode
Serial	H	CSB	L	4-pin SPI mode
	L			3-pin SPI mode

Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in table 10. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table 11.

Table 10. Microprocessor Selection for Parallel Interface

PS1	CSB	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	RS	E	RW	DB0 to DB7	6800-series
L	CSB	RS	/RD	/WR	DB0 to DB7	8080-series

Table 11. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When E_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at RS, RW_WR as in case of 6800-series mode.

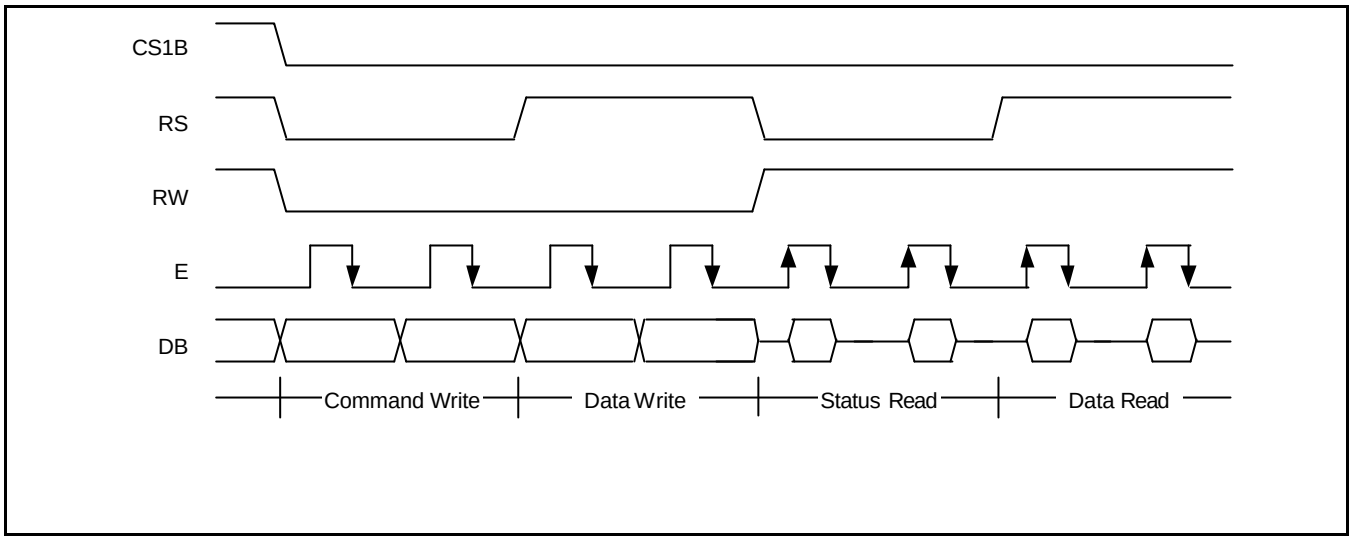


Figure 5. 6800-Series MPU Interface protocol (PS="H", MI="H")

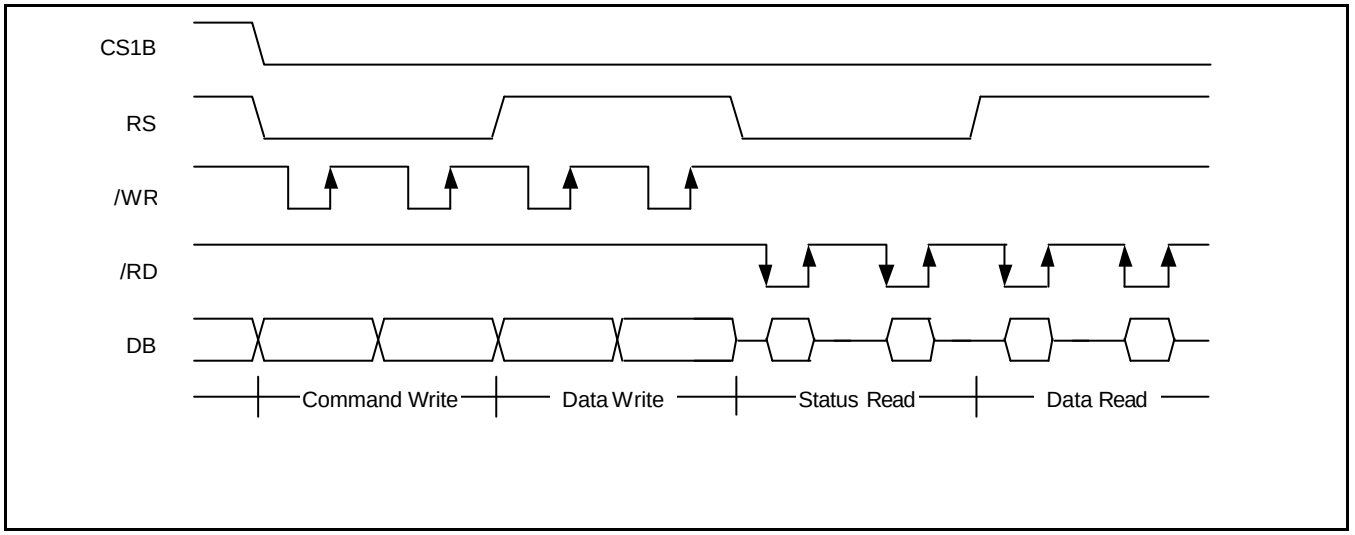


Figure 6. 8080-Series MPU Interface Protocol (PS="H", MI="L")

Serial Interface (PS0 = "L")

When the S6B0729 is active (CSB="L"), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select(RS) Pin, based on the setting of PS1. When the RS pin is used (PS1 = "H"), data is display data when RS is high, and command data when RS is low. When RS is not used (PS1 = "L"), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are send, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

Serial mode	PS0	PS1	CSB	RS
4-Pin SPI mode	L	H	CSB	Used
3-Pin SPI mode	L	L	CSB	Not used

4-pin SPI Mode (PS0 = "L" , PS1 = "H")

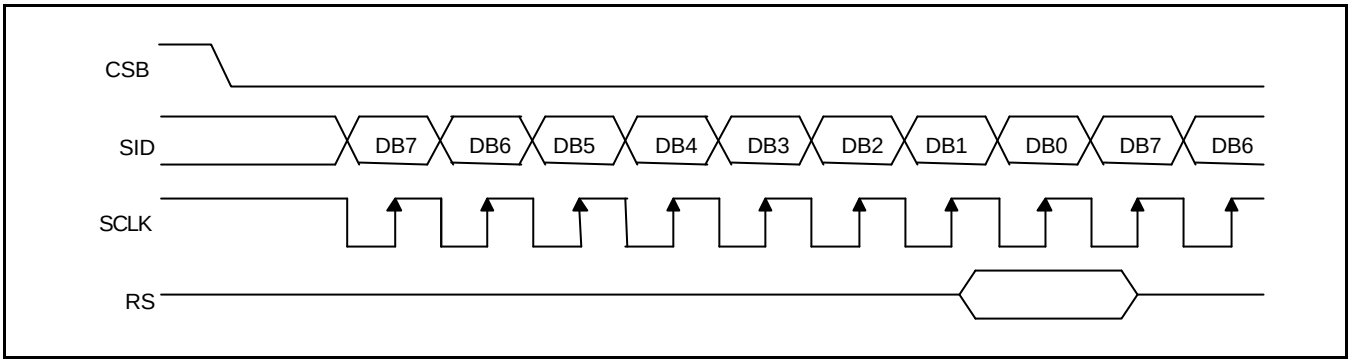
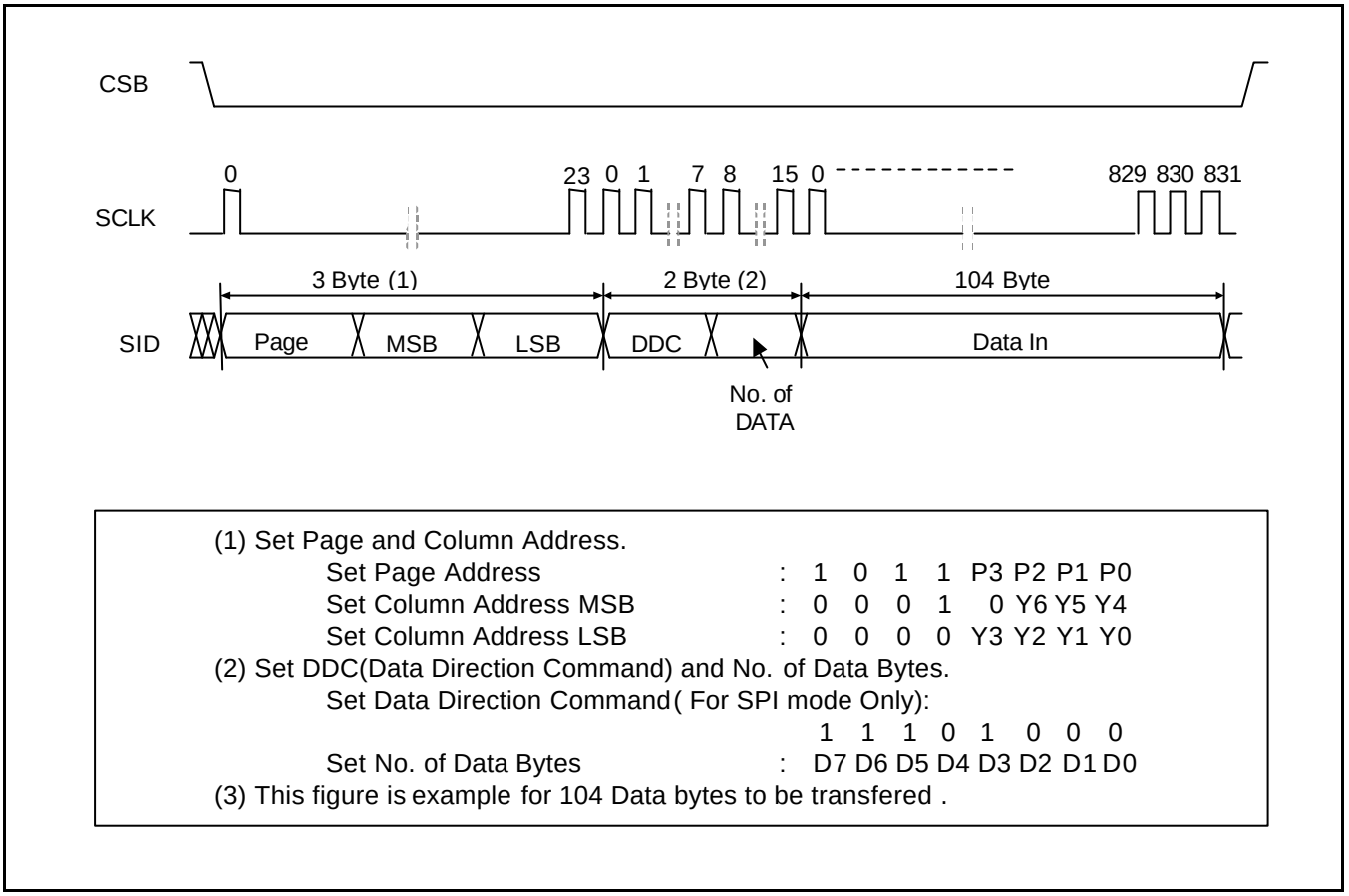


Figure 2. 4-pin SPI Timing (RS is used)

3-pin SPI Mode (PS0 = "L" , PS1 = "L")

To write data to the DDRAM, send Data Direction Command in 3-pin SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.



(1) Set Page and Column Address.

Set Page Address	:	1	0	1	1	P3	P2	P1	P0
Set Column Address MSB	:	0	0	0	1	0	Y6	Y5	Y4
Set Column Address LSB	:	0	0	0	0	Y3	Y2	Y1	Y0

(2) Set DDC(Data Direction Command) and No. of Data Bytes.

Set Data Direction Command (For SPI mode Only):

	1	1	1	0	1	0	0	0
Set No. of Data Bytes :	D7	D6	D5	D4	D3	D2	D1	D0

(3) This figure is example for 104 Data bytes to be transfered .

Figure 3. 3-pin SPI Timing (RS is not used)

This command is used in 3-pin SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

Busy Flag

The Busy Flag indicates whether the S6B0729 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0729 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 5. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 6. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

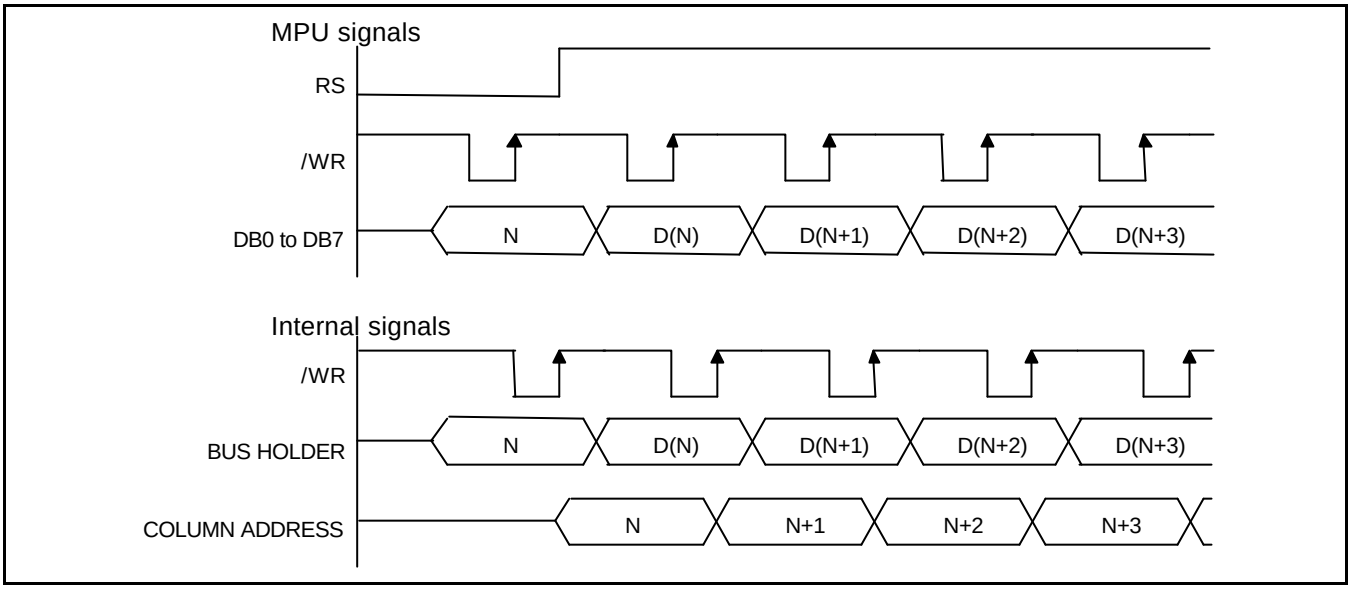


Figure 4. Write Timing

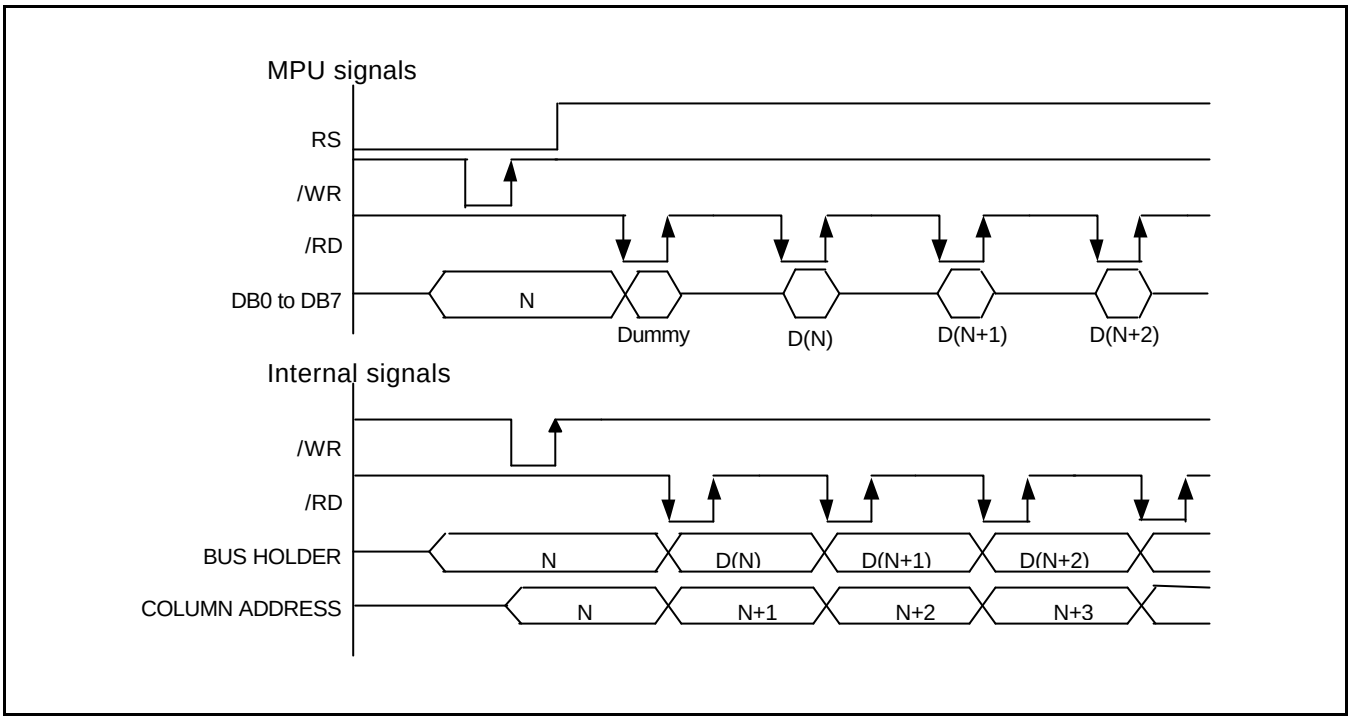


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 81-row (10 page by 8 bits & icon page by 1 bit) by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page address 11 is a special RAM area for the icons and display data DB0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 102-bit RAM data to the display data latch circuit.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 7-bit [Y7:Y1] are set and lowest bit, Y0 is set to "0". Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 65H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address counter.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

SEG output	SEG 0		SEG 1		SEG 2		SEG 3		... ...	SEG 98		SEG 99		SEG 100		SEG 101	
Column address [Y7:Y1]	00H		01H		02H		03H		... ...	62H		63H		64H		65H	
Internal column address [Y7:Y0]	00 HEX	01 HEX	02 HEX	03 HEX	04 HEX	05 HEX	06 HEX	07 HEX	... ...	C4 HEX	C5 HEX	C6 HEX	C7 HEX	C8 HEX	C9 HEX	CA HEX	CB HEX
Display data (ADC = 0)	1	1	1	0	0	0	0	1	... ...	1	0	1	1	0	0	0	1
LCD panel display									... ...								
Display data (ADC = 1)	0	1	0	0	1	1	1	0	... ...	0	1	0	0	1	0	1	1
LCD panel display									... ...								

Figure 7. The Relationship between the Column Address and The Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

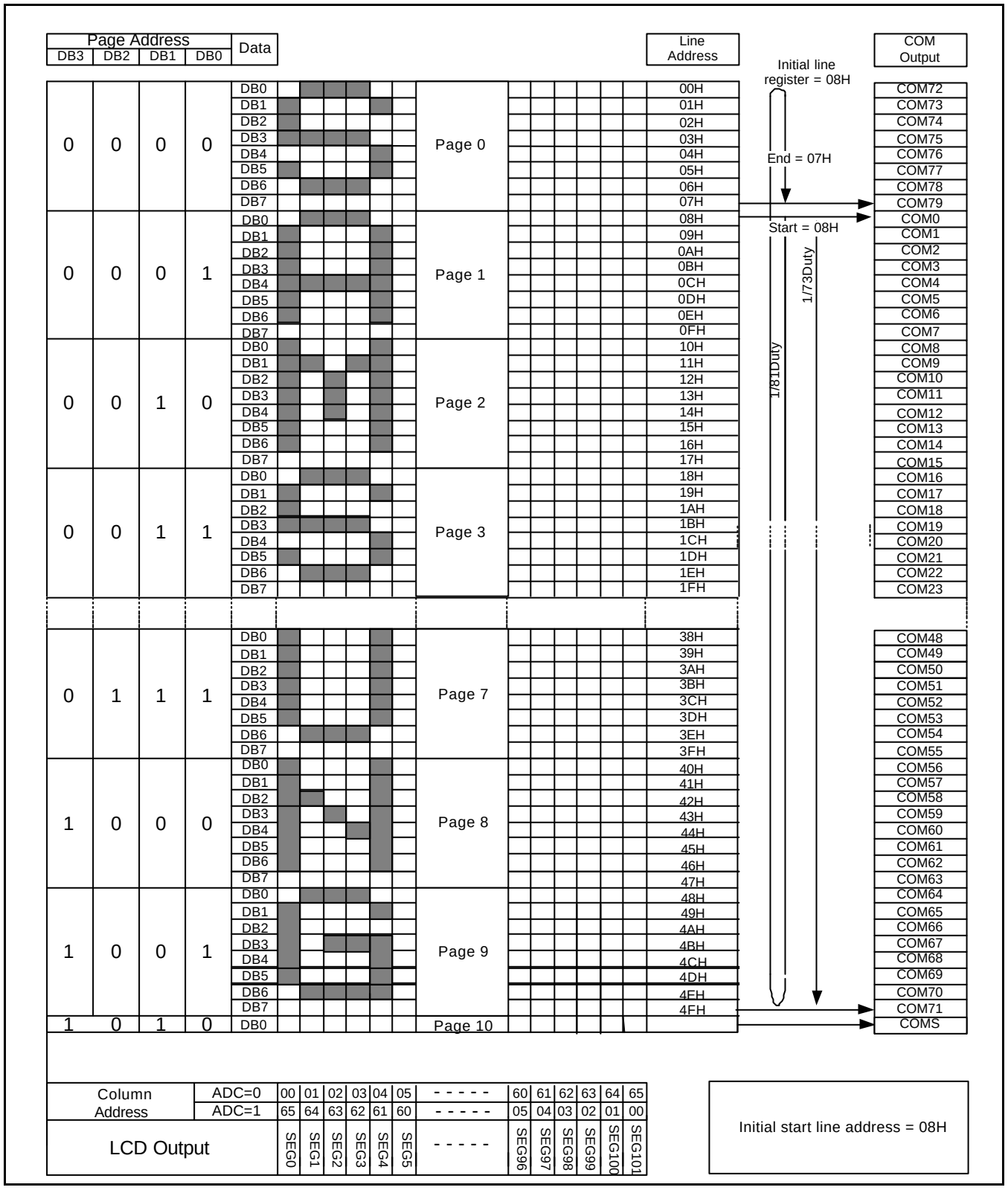


Figure 8. Display Data RAM Map

LCD DISPLAY CIRCUITS

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The S6B0729 incorporates an FRC function and a PWM function circuit to display a 4-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The S6B0729 provides four 4-bit palette-registers to assign the desired gray level. These registers are set by the instructions and the RESETB.

– **Gray Scale Table of 4 FRC (Frame Rate Control)**

Gray scale level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

– **Gray Scale Table of 3 FRC (Frame Rate Control)**

Gray scale level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)

– **Gray Scale Table of 15 PWM (Pulse Width Modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/15)	Brighter
1	01	0001	1/15	
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	
11	0B	1011	11/15	
12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1 (15/15)	Darker

– **Gray Scale Table of 12 PWM (Pulse Width Modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1 (12/12)	Darker
13	0D	1101	0/12	This area is selected to OFF level (0/12 level)
14	0E	1110	0/12	
15	0F	1111	0/12	

– **Gray Scale Table of 9 PWM (Pulse Width Modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/9)	Brighter
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1 (9/9)	Darker
10	0A	1010	0/9	This area is selected to OFF level (0/9 level)
11	0B	1011	0/9	
12	0C	1100	0/9	
13	0D	1101	0/9	
14	0E	1110	0/9	
15	0F	1111	0/9	

Oscillator

This is on-chip Oscillator with external resistor. Its frequency is controlled by external resistor between OSC1 and VDD. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL(internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 102-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 9.

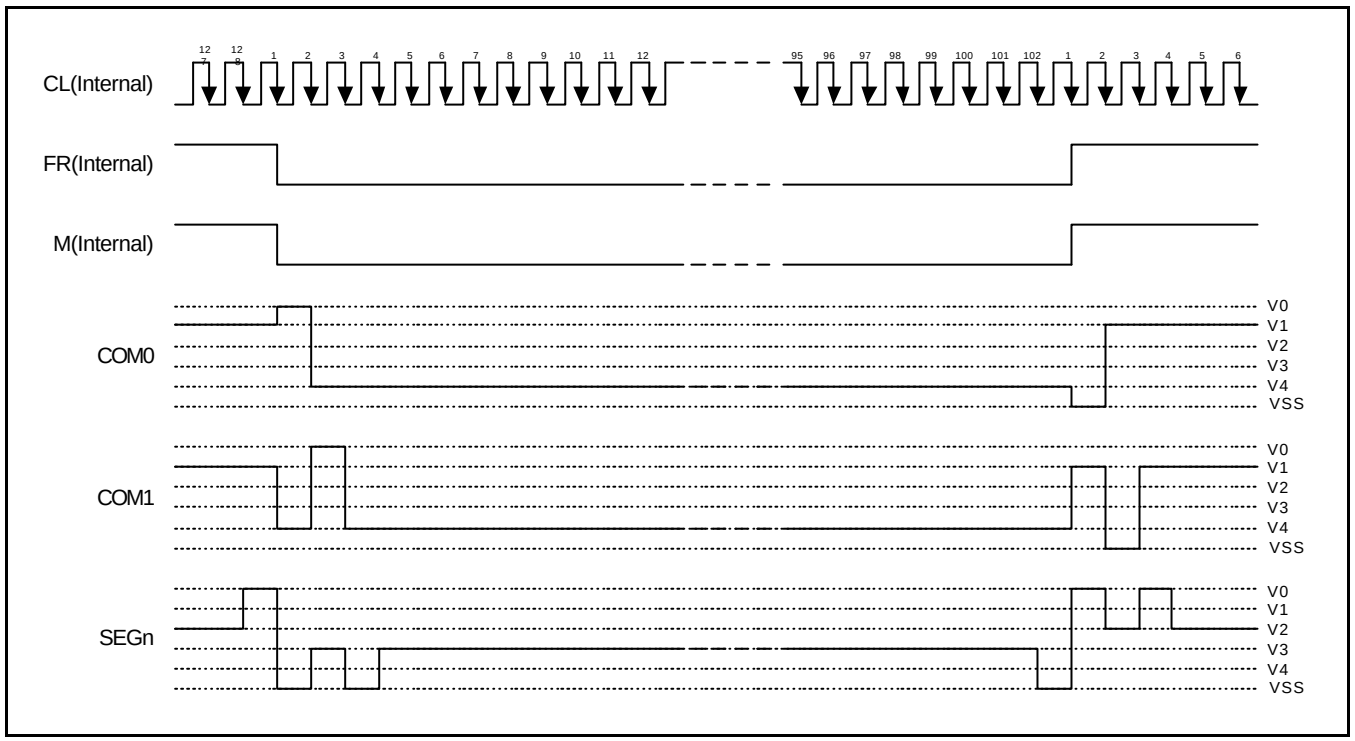


Figure 9. 2-frame AC Driving Waveform (Duty Ratio = 1/102)

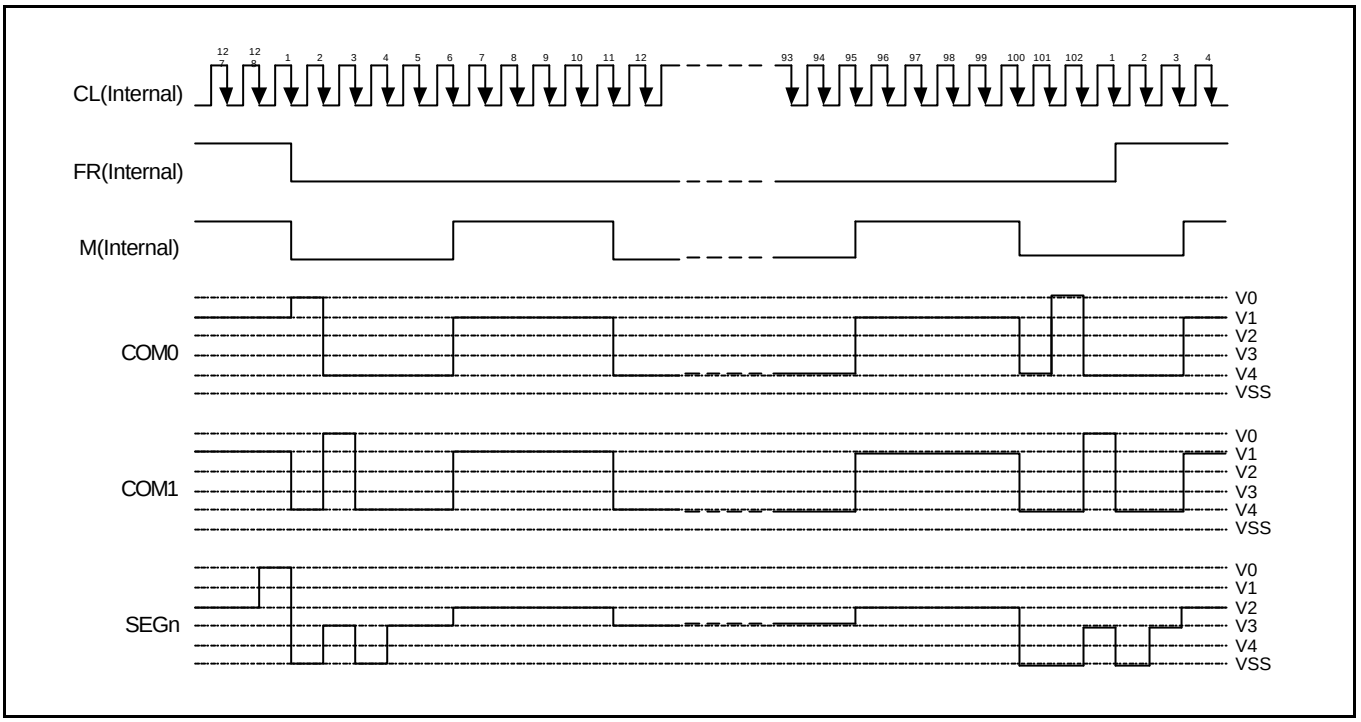


Figure 10. N-Line Inversion Driving Waveform (N = 5, Duty Ratio = 1/102)

LCD DRIVER CIRCUIT

This driver circuit is configured by 81-channel common drivers and 102-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

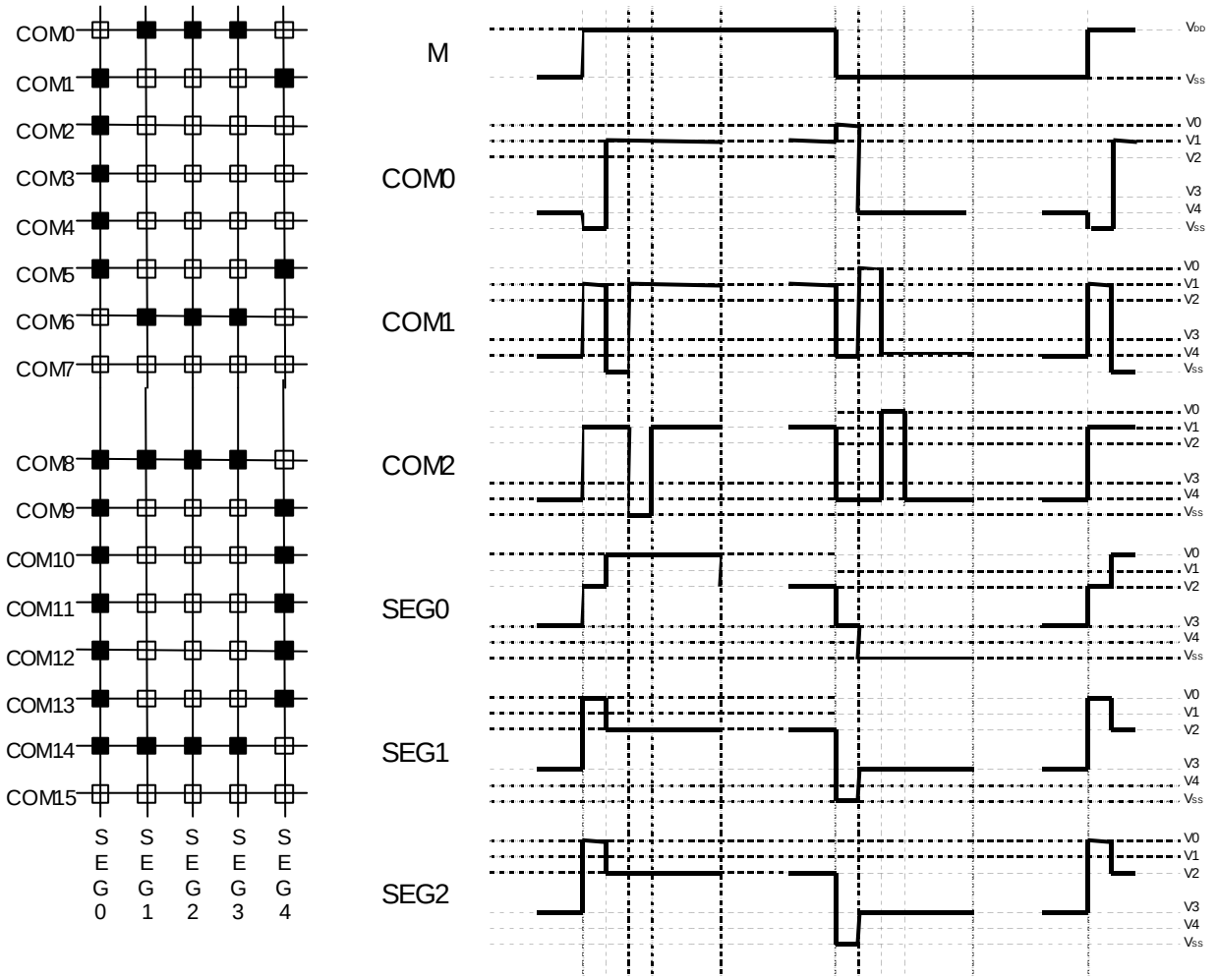


Figure 11. Segment and Common Timing

Partial Display on LCD

The S6B0729 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

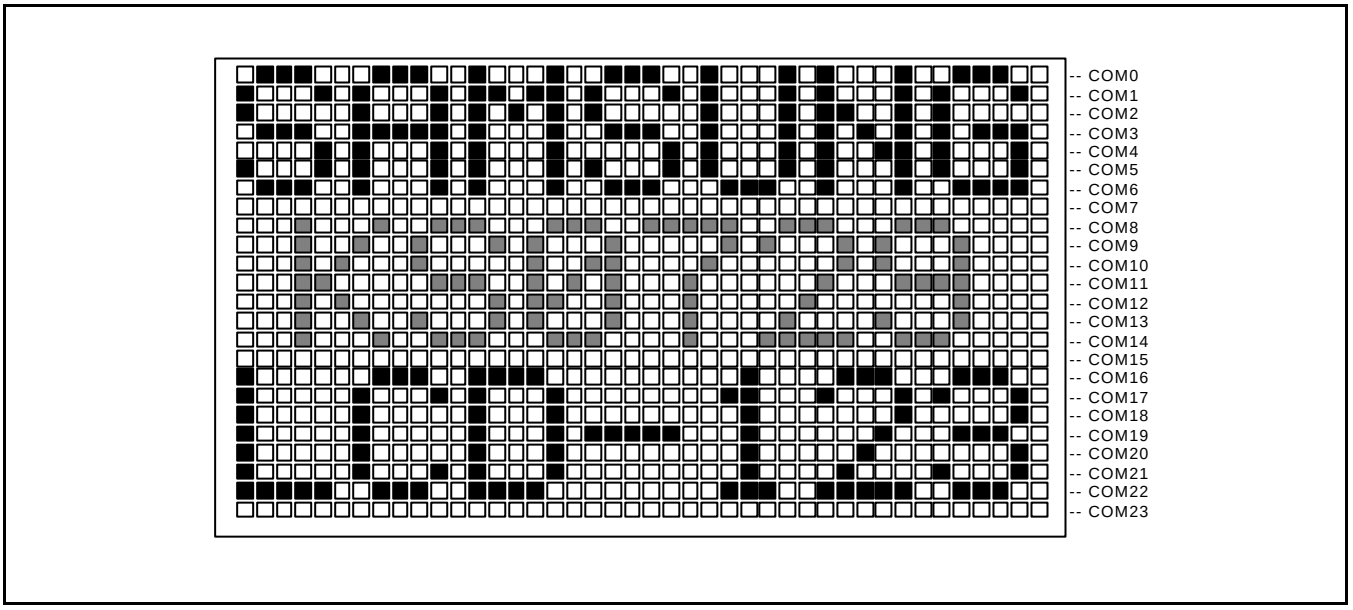


Figure 12. Reference Example for Partial Display

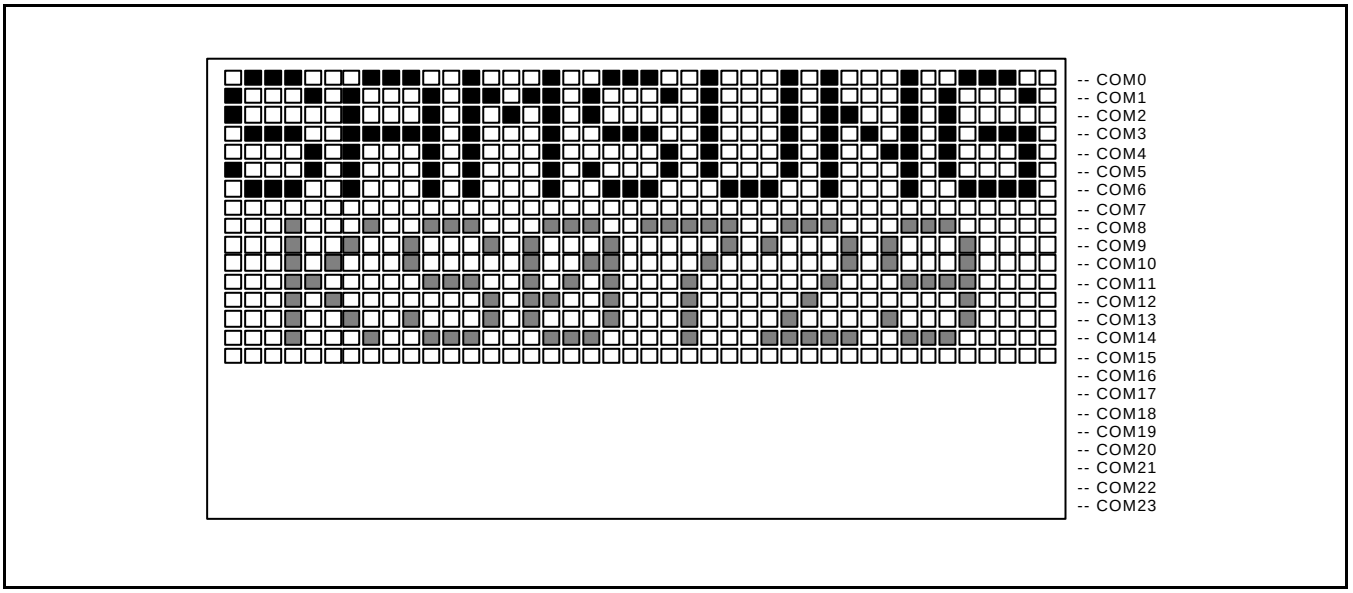


Figure 13. Partial Display (Partial Display Duty = 16, Initial COM0 = 0)

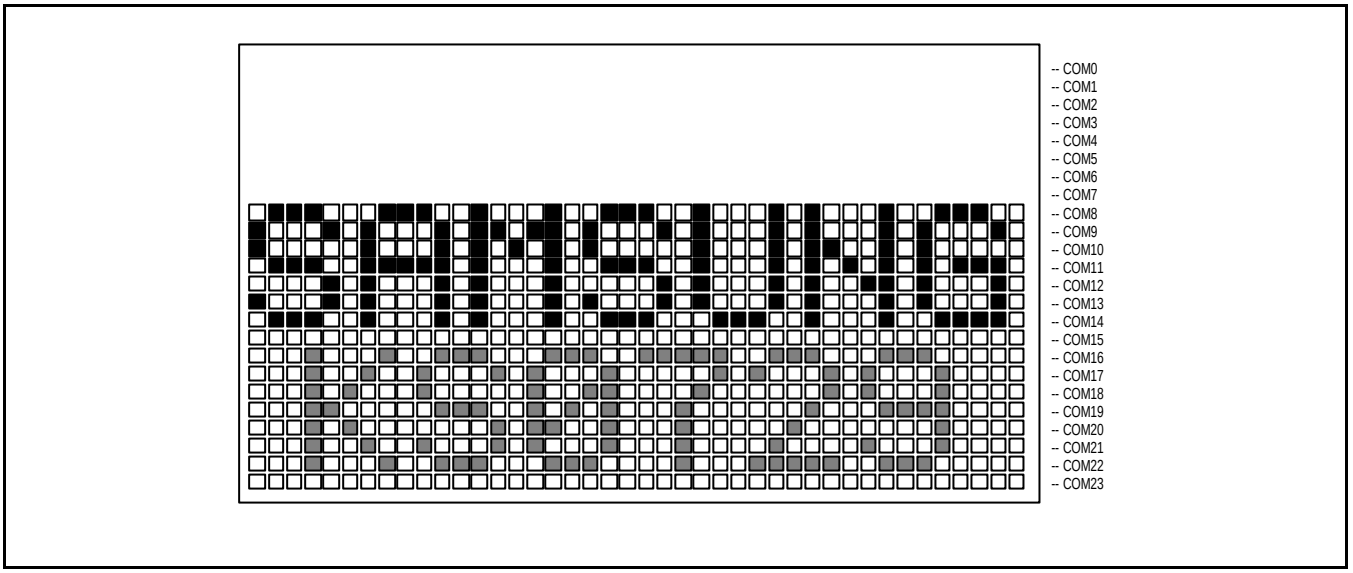


Figure 14. Moving Display (Partial Display Duty = 16, Initial COM0 = 8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 12 shows the referenced combinations in using Power Supply circuits.

Table 12. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 μF]

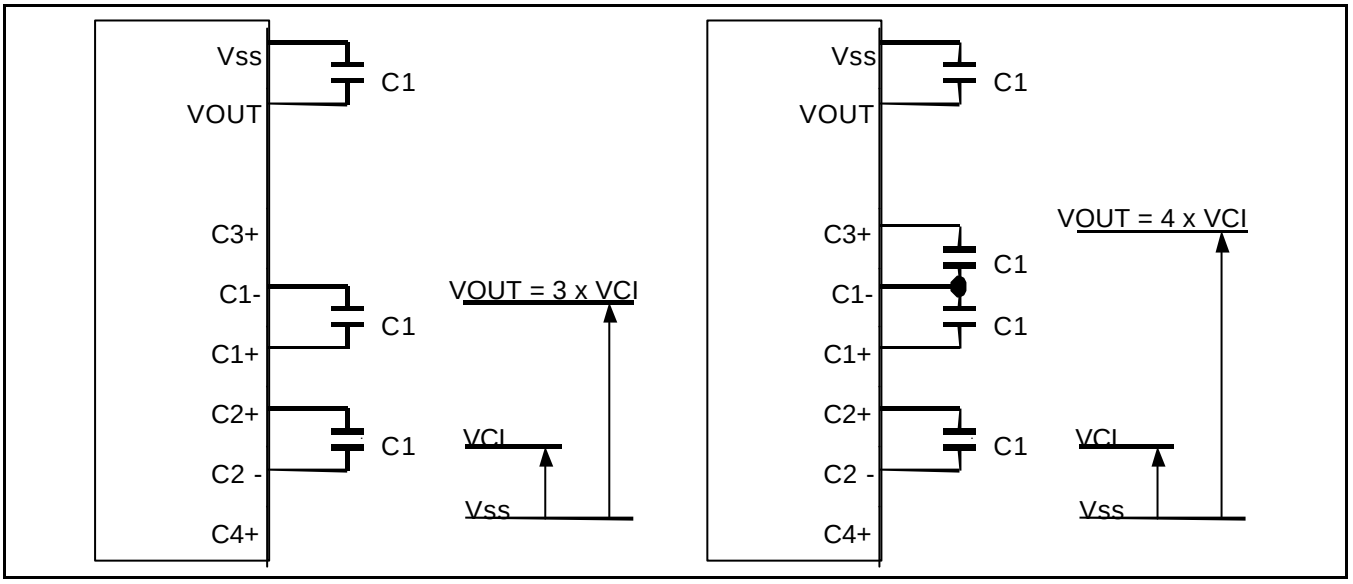


Figure 15. Three Times Boosting Circuit **Figure 16. Four Times Boosting Circuit**

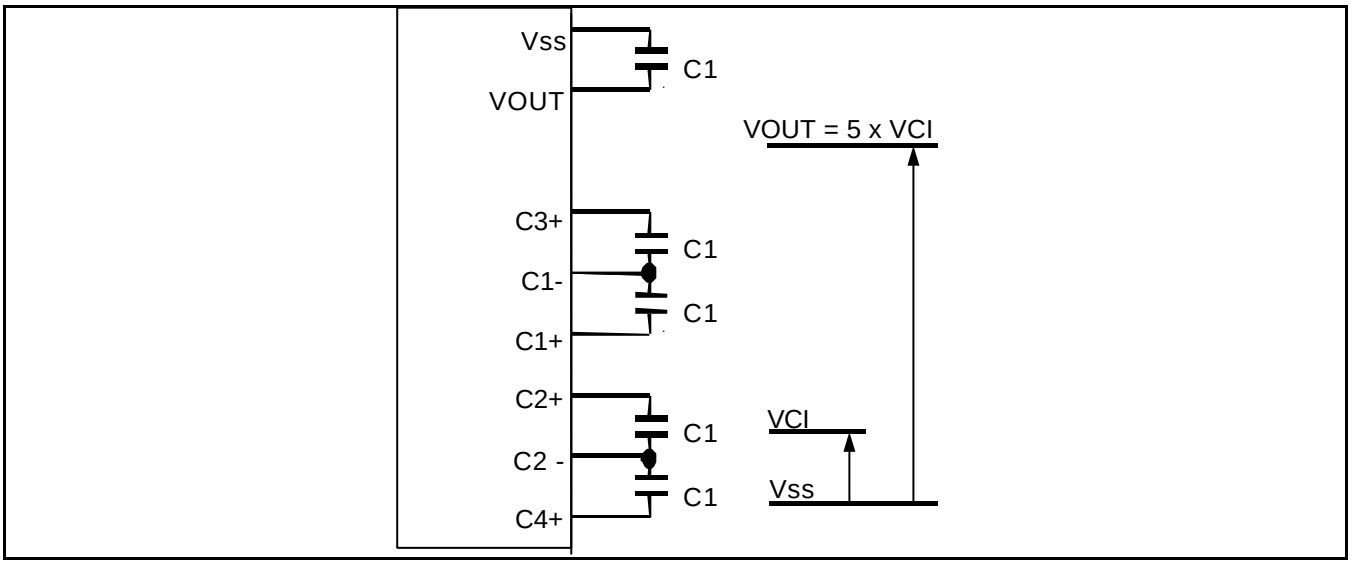


Figure 17. Five Times Boosting Circuit

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure18, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta= 25°C is shown in Table 13.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{210}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 13 . V_{REF} Voltage at Ta = 25°C

REF	Temp. coefficient	V_{REF} [V]
1	-0.125% / °C	2.1
0	External input	VEXT

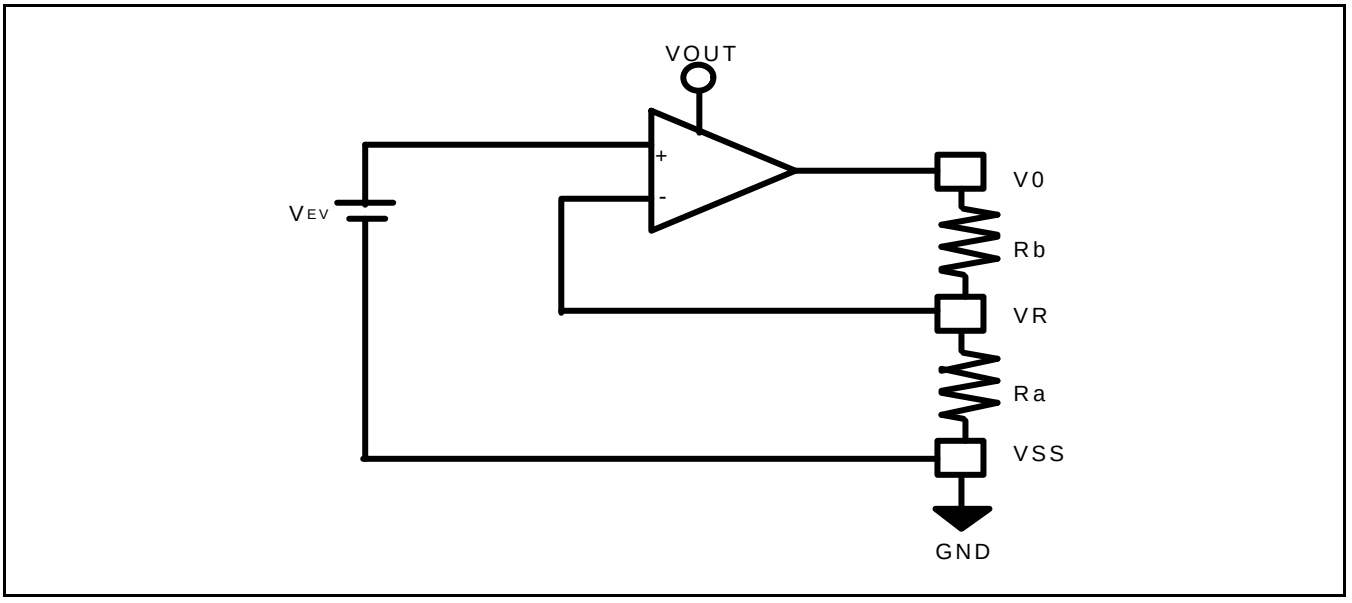


Figure 18. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is **"H"**, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 14. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Figure19 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

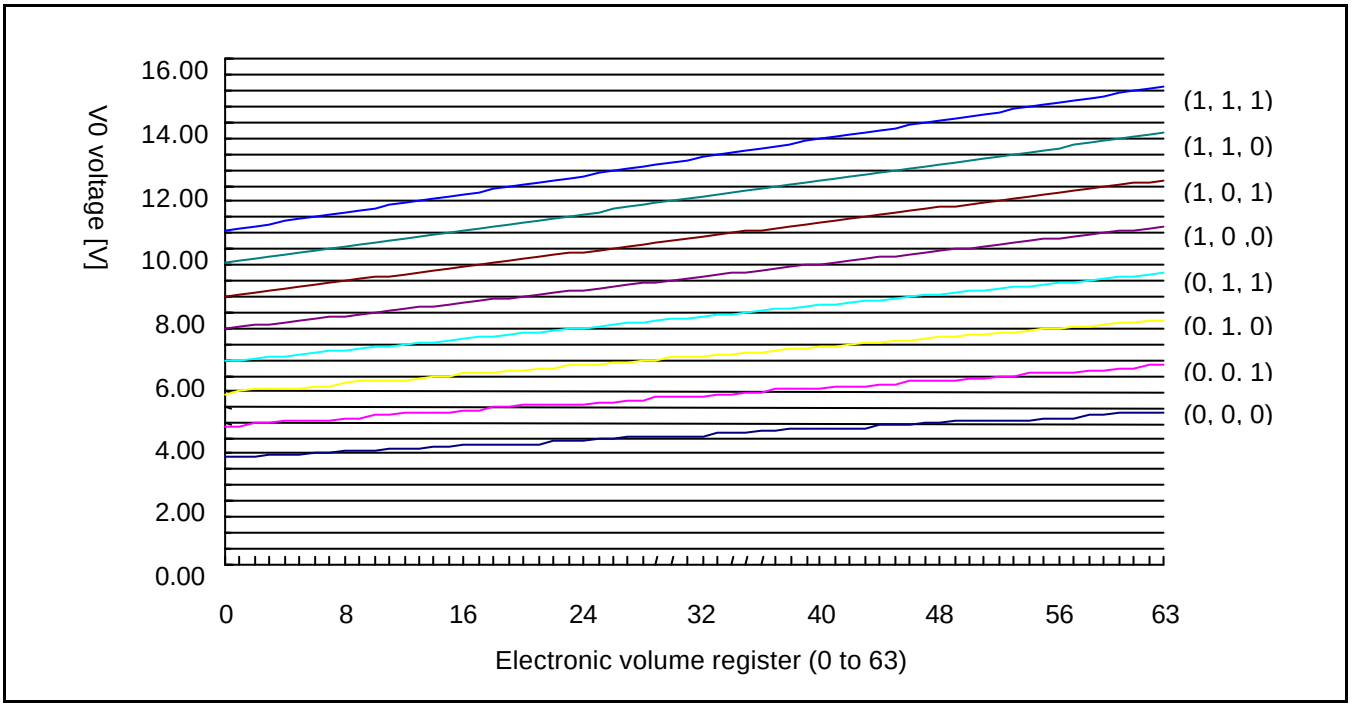


Figure19. Electronic Volume Level (Temp. Coefficient = -0.125% / °C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 1

$$V_{EV} = \left(1 - \frac{(63 - 32)}{210}\right) \times 2.1 = 1.79 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \ [uA] \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5

Ra = 1.79 [MΩ]

Rb = 8.21 [MΩ]

Table 15 Shows the Range of V0 depending on the above Requirements.

Table 15. The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.21	.....	10.00	.....	11.73

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 16 shows the relationship between V1 to V4 level and each duty ratio.

Table 16. The Relationship between V1 to V4 Level and Each Duty Ratio

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-2)/N x V0	2/N x V0	1/N x V0	N = 4,5,9,10

DISCHARGE CIRCUIT

When Power save mode instruction is executed or the power supply switched off, the VLCD voltages(V0,V1,V2,V3,V4) are discharged forcibly by this circuit.

REFERENCE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [µF], C2 = 0.47 to 2.0 [µF]]

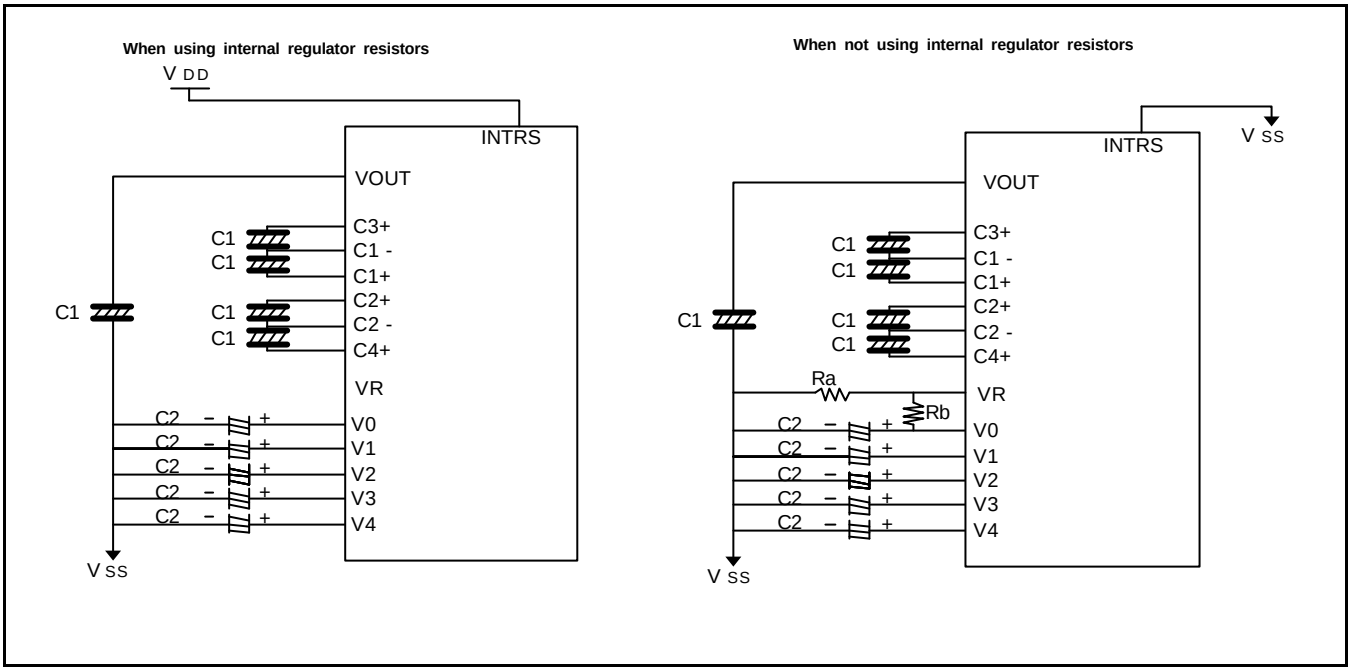


Figure 20. When Using all LCD Power Circuits (5-Time V/C: ON, V/R: ON, V/F: ON)

[C2 = 0.47 to 2.0 [µF]]

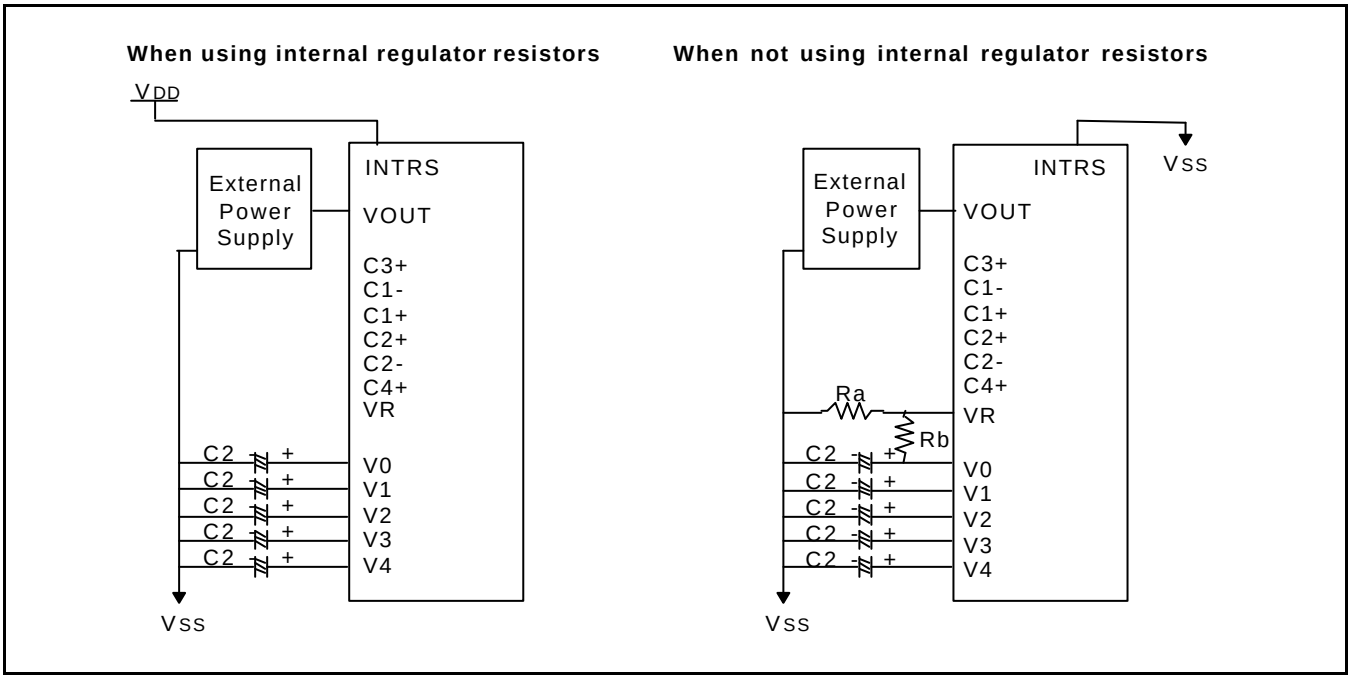


Figure 21. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

[C2 = 0.47 to 2.0 [µF]]

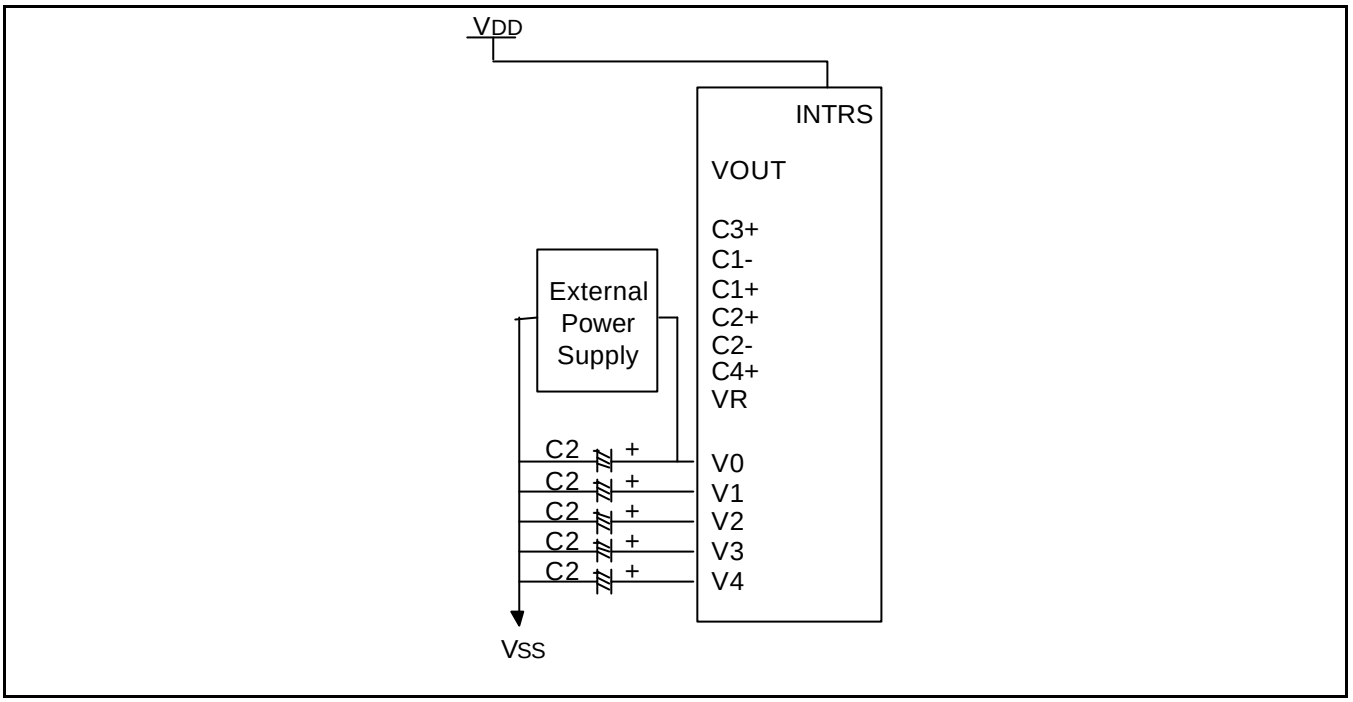


Figure 22. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

[C2 = 0.47 to 2.0 [µF]]

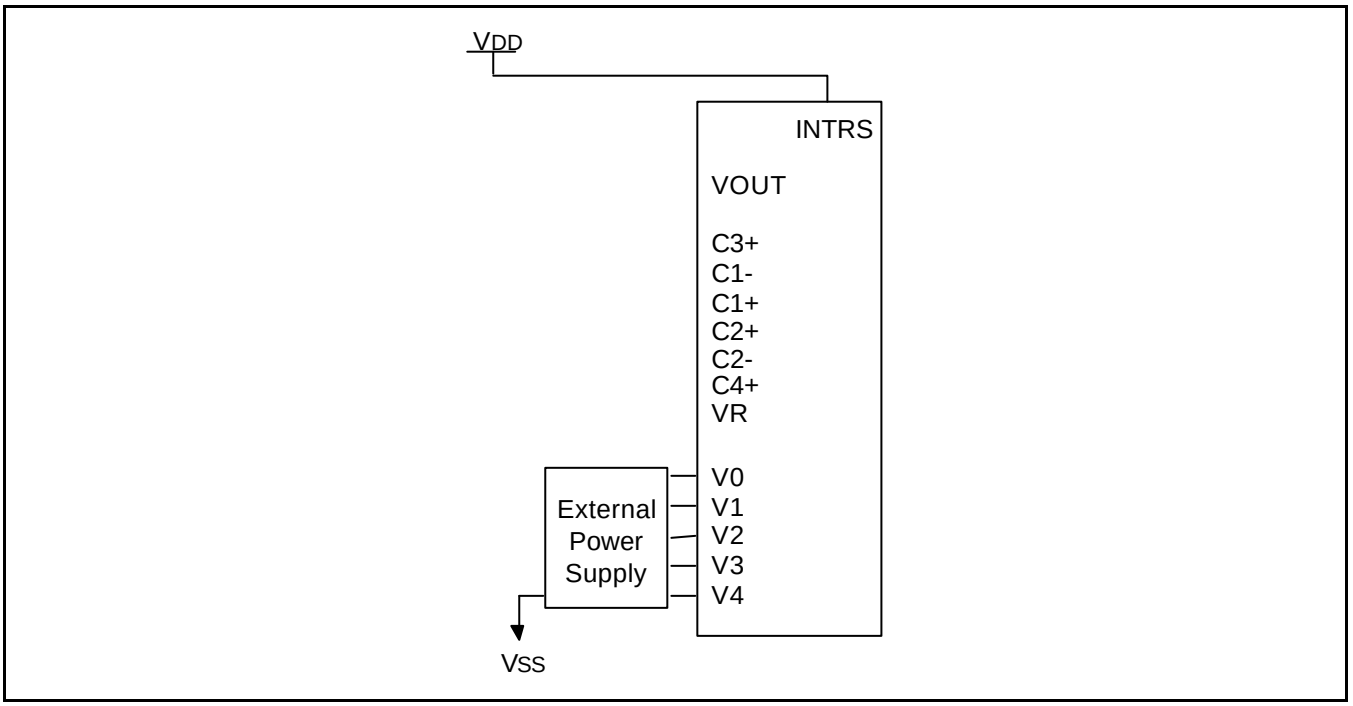


Figure 23. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

Page address: 0
Column address: 0
Read-modify-write: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/80
Reverse display ON / OFF: OFF (normal)
N-line inversion register: 0 (disable)
Entire Display ON/OFF: OFF
ICON Control register ON/OFF: OFF (ICON disable)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC converter circuit = (0, 0)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
LCD bias ratio: 1/9
COM Scan Direction: 0
ADC Select: 0
Oscillator: OFF
Power Save Mode: Release
Display Data Length register: 0 (for SPI mode)
White mode set: OFF
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
Light gray mode set: OFF
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
Dark gray mode set: OFF
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
Black mode set: OFF
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
FRC, PWM mode: 4FRC, 9PWM

When RESET instruction is issued, following procedure is occurred.

Page address: 0
Column address: 0
Read-modify-write: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
Display Data Length register: 0 (for SPI mode)
White mode set: OFF
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
Light gray mode set: OFF
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
Dark gray mode set: OFF
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
Black mode set: OFF
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
FRC, PWM mode: 4FRC, 9PWM

While RESETB is "L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 17. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable (default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: display OFF D=1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial display duty ratio
	0	0	×	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set N-line inversion register
	0	0	×	×	×	N4	N3	N2	N 1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line Inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display, REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display. EON=1: entire display ON

Table 17. Instruction Table (Continued)

× : Don' t care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the Reference voltage
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
Set data direction & display data length(DDL)	×	×	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI Mode)
	×	×	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0	0	1	1	1	0	0	0	1	1	*No operation*
Test Instruction	0	0	1	1	1	1	×	×	×	×	*Don't use this instruction.*

Table 17. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM
Set white mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	0	0	0	Set white mode and 1st/2nd frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	
Set white mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	0	0	1	Set white mode and 3rd/4th frame
	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	
Set light gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	0	1	0	Set light gray mode and 1st/2nd frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	
Set light gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	0	1	1	Set light gray mode and 3rd/4th frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	
Set dark gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	0	0	Set dark gray mode and 1st/2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	
Set dark gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	0	1	Set dark gray mode and 3rd/4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	
Set black mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	1	0	Set black mode and 1st/2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	
Set black mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	1	1	Set black mode and 3rd/4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

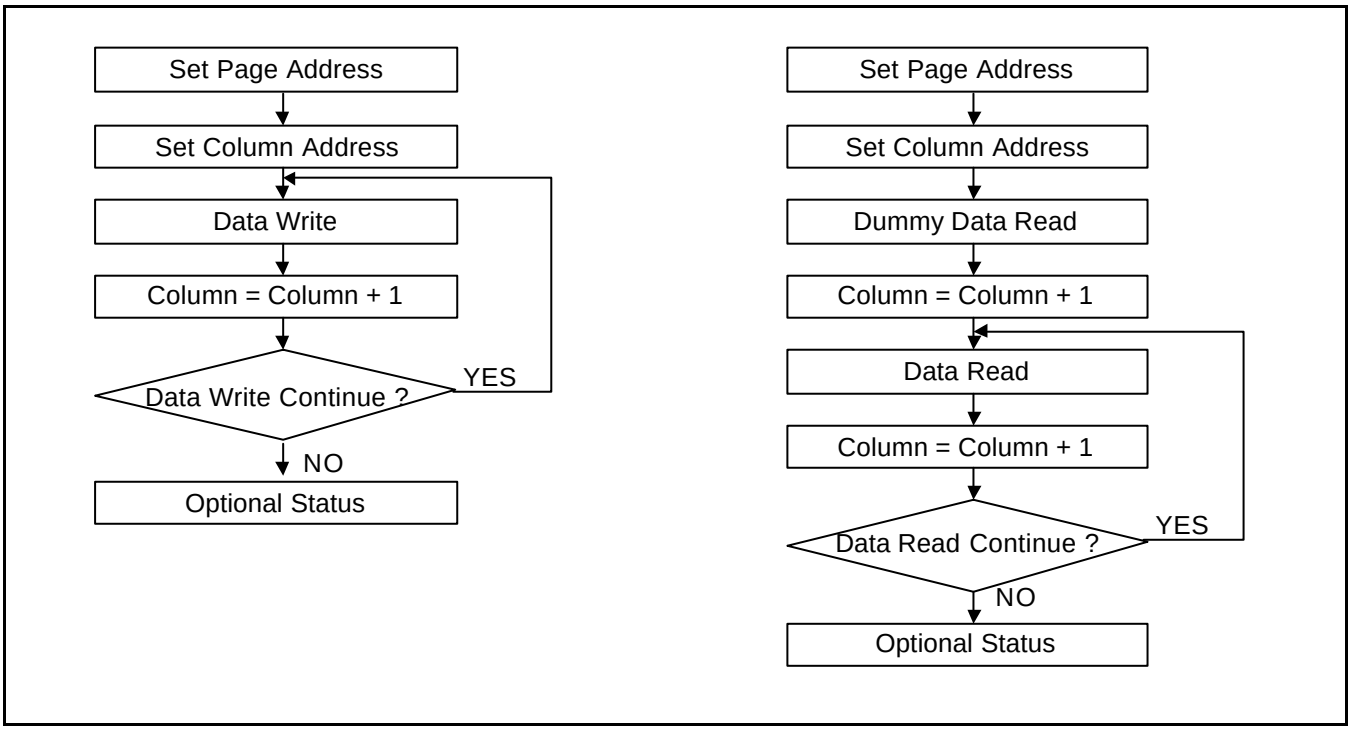


Figure 24. Sequence for Writing Display Data

Figure 25. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B0729

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON / OFF	RES	MF2	MF1	MF0	DS1	DS0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ON / OFF	Indicates display ON / OFF status 0: display OFF, 1: display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID, MF2 MF1 MF0 = [0 0 0]
DS	Display size ID, DS1 DS0 = [1 0]

ICON Control Register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible to set the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, ICON display is disabled.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)
ICON=1: ICON enable & set the page address to 16

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status. Set Page Address instruction can not be used to set the page address to "10". Use ICON control register ON/OFF instruction to set the page address to "10".

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	0	0	1	9
1	0	1	0	10

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

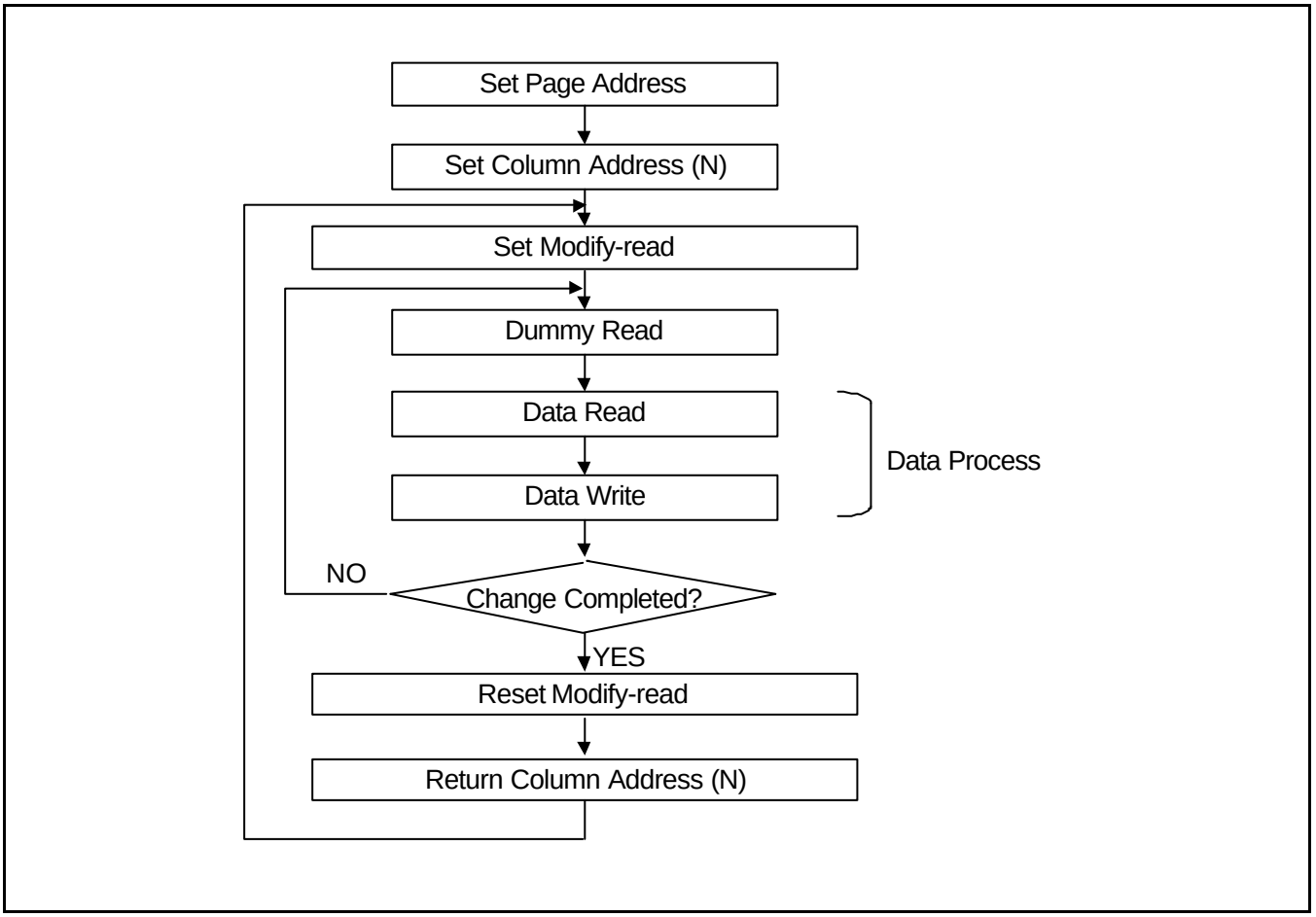


Figure 26. Sequence for Cursor Display

Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79
1	0	1	0	0	0	0	
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

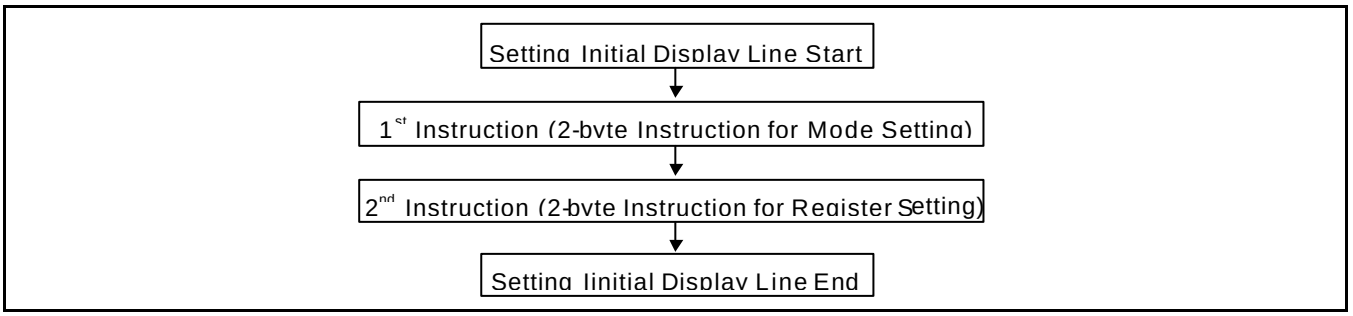


Figure 27. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	0	0	1	1	0	0	COM76
1	0	0	1	1	0	1	COM77
1	0	0	1	1	1	0	COM78
1	0	0	1	1	1	1	COM79

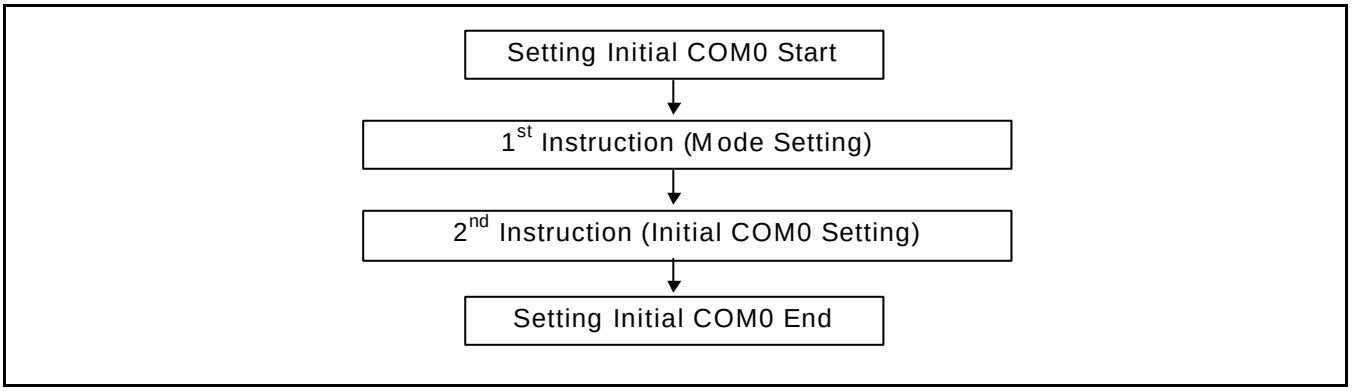


Figure 28. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 80 (ICON disabled) or 17 to 81 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	D6	D5	D4	D3	D2	D1	D0

D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio (ICON disabled)	Selected partial duty ratio (ICON enabled)
0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:		
0	0	0	1	1	1	1		
0	0	1	0	0	0	0	1/16	1/17
0	0	1	0	0	0	1	1/17	1/18
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1/79	1/80
1	0	1	0	0	0	0	1/80	1/81
1	0	1	0	0	0	1	No operation	No operation
:	:	:	:	:	:	:		
1	1	1	1	1	1	1		

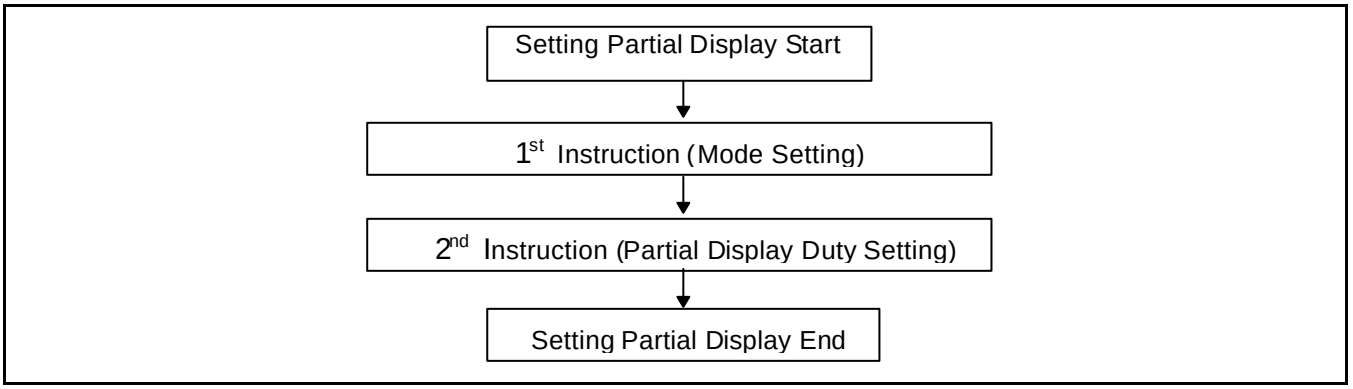


Figure29. Sequence for Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D : The number of display duty ratio (D is selectable by customers)
N : N for N-line inversion (N is selectable by customers).

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

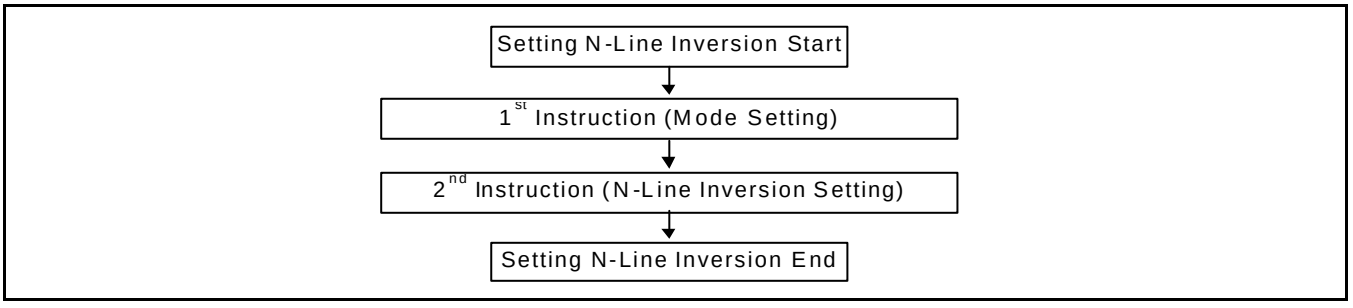


Figure 30. Sequence for N-line Inversion

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Dark
0 (normal)	White ("00")	Light gray ("01")	Dark gray ("10")	Dark ("11")
1 (reverse)	Dark ("11")	Dark gray ("10")	Light gray ("01")	White ("00")

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Dark
0 (normal)	White ("00")	Light gray ("01")	Dark gray ("10")	Dark ("11")
1 (entire)	Dark ("11")	Dark ("11")	Dark ("11")	Dark ("11")

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Select DC-DC Step-up

Selects one of 3 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit

Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 14.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set Electronic Volume Register

Consist of 2-byte Instructions
The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

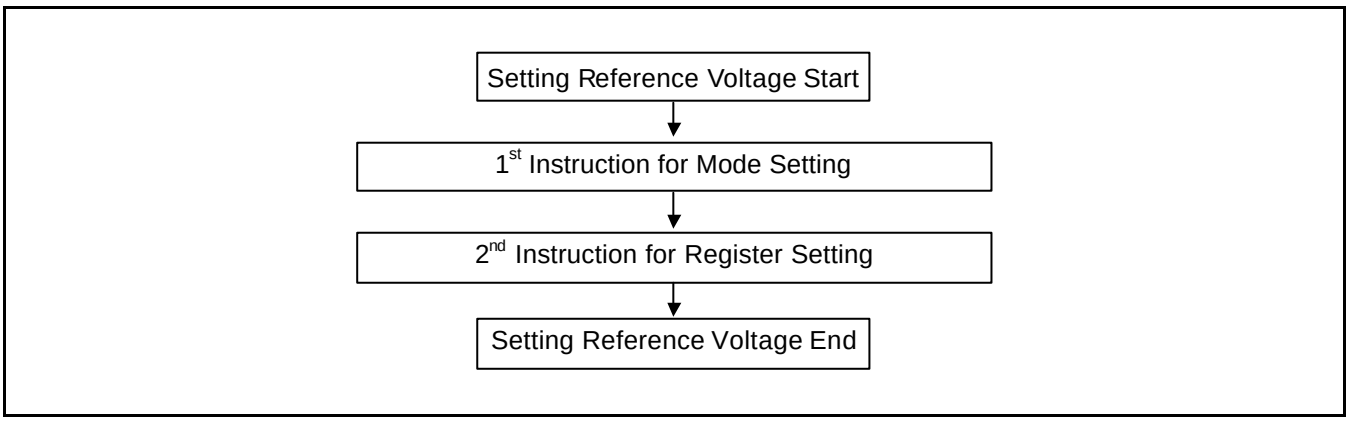


Figure 31. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6-
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/10

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

×: Don't care

SHL = 0: normal direction (COM0 → COM79)
SHL = 1: reverse direction (COM79 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG101)
ADC = 1: reverse direction (SEG101 → SEG0)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power Save

The S6B0729 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode
P = 1: sleep mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

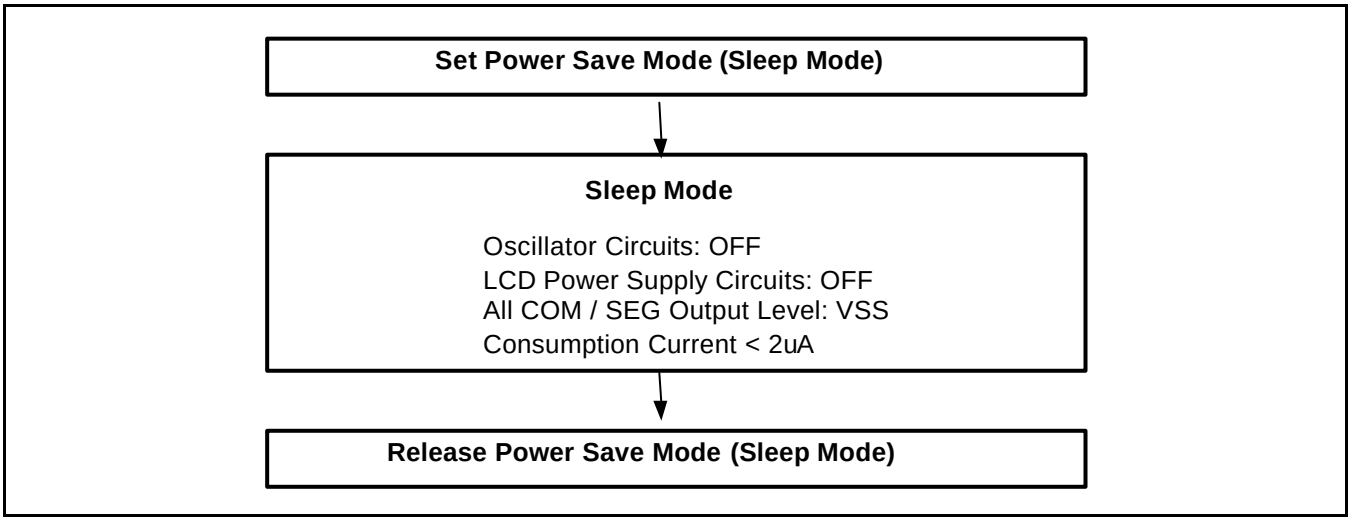


Figure 32. Power Save Routine

Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set Data Direction & Display Data Length (3-Pin SPI Mode)

Consists of 2 bytes instruction.
This command is used in 3-Pin SPI mode only(PS0 = "L" and PS1 = "L"). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOP

No operation

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

Set PWM & FRC mode

Selects 3/4 FRC and 9 / 12 / 15 PWM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	9PWM
	0	1	9PWM
	1	0	12PWM
	1	1	15PWM

Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

– **Set Gray Scale Mode**

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM2	GM1	GM0	Description
0	0	0	In case of setting white mode and 1st / 2nd frame
0	0	1	In case of setting white mode and 3rd / 4th frame
0	1	0	In case of setting light gray mode and 1st / 2nd frame
0	1	1	In case of setting light gray mode and 3rd / 4th frame
1	0	0	In case of setting dark gray mode and 1st / 2nd frame
1	0	1	In case of setting dark gray mode and 3rd / 4th frame
1	1	0	In case of setting black mode and 1st / 2nd frame
1	1	1	In case of setting black mode and 3rd / 4th frame

– **Set Gray Scale Register**

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Pulse width (9PWM)	Pulse width (12PWM)	Pulse width (15PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	1	1/9	1/12	1/15
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	1	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

∗ GA3=WA3,LA3,DA3,BA3 GA2=WA2,LA2,DA2,BA2 GA1=WA1,LA1,DA1,BA1 GA0=WA0,LA0,DA0,BA0
GB3=WB3,LB3,DB3,BB3 GA2=WB2,LB2,DB2,BB2 GA1=WB1,LB1,DB1,BB1 GA0=WB0,LB0,DB0,BB0
GC3=WC3,LC3,DC3,BC3 GA2=WC2,LC2,DC2,BC2 GA1=WC1,LC1,DC1,BC1 GA0=WC0,LC0,DC0,BC0
GD3=WD3,LD3,DD3,BD3 GA2=WD2,LD2,DD2,BD2 GA1=WD1,LD1,DD1,BD1 GA0=WD0,LD0,DD0,BD0

Referential Instruction Set-up Flow: Initializing with the built-in Power Supply Circuits

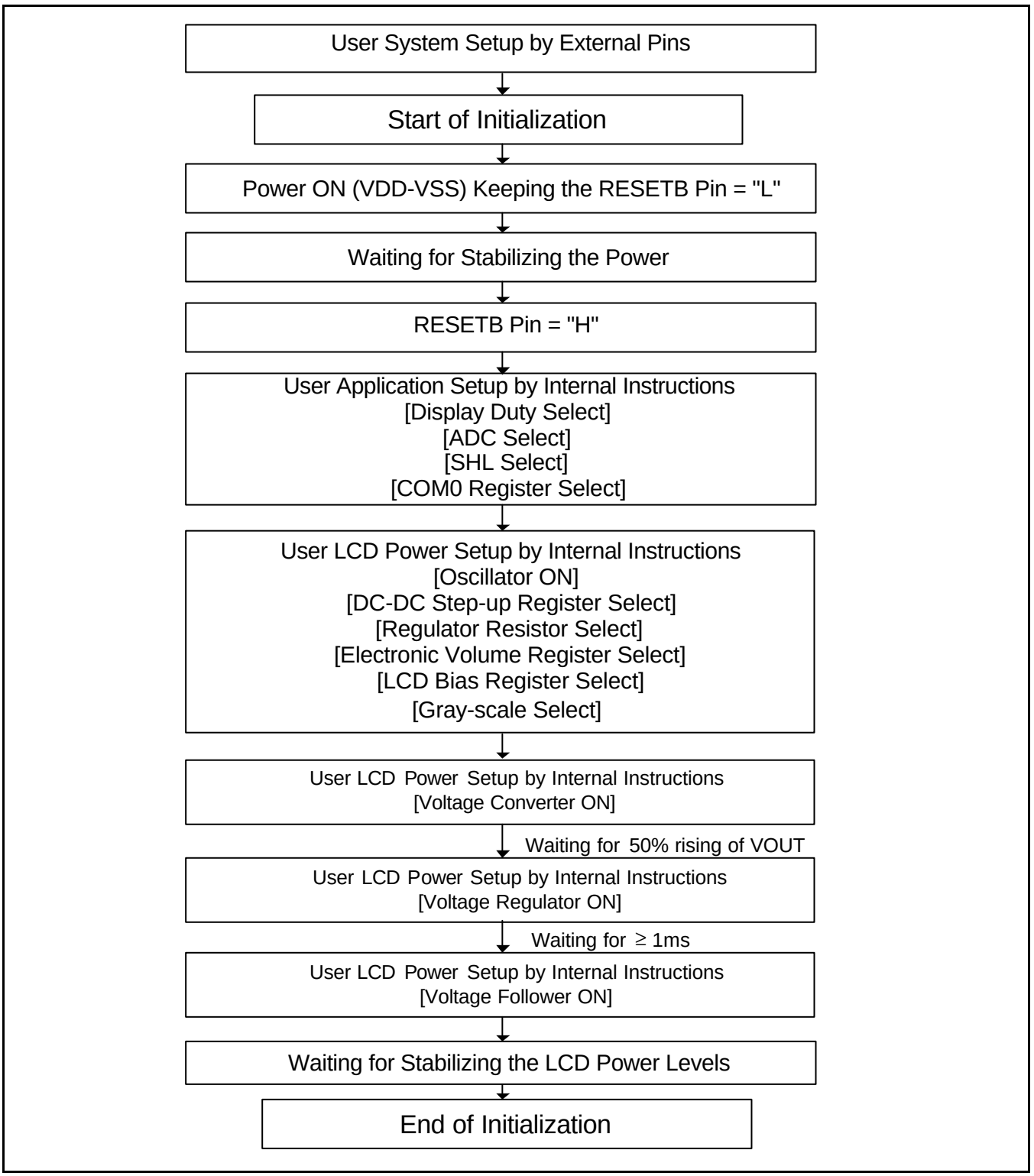


Figure 33. Initializing with the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Initializing without the built-in Power Supply Circuits

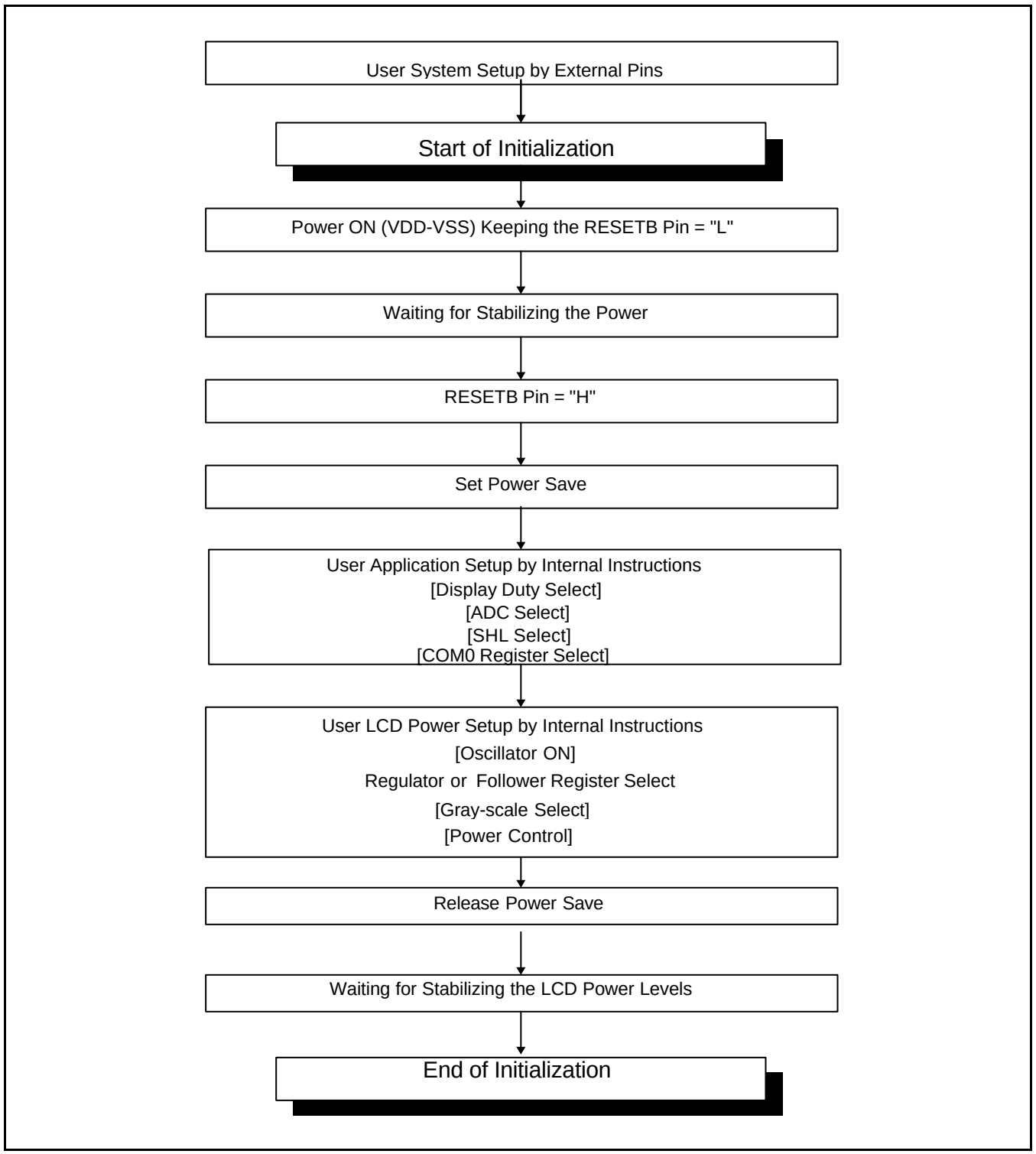


Figure 34. Initializing without the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Data Displaying

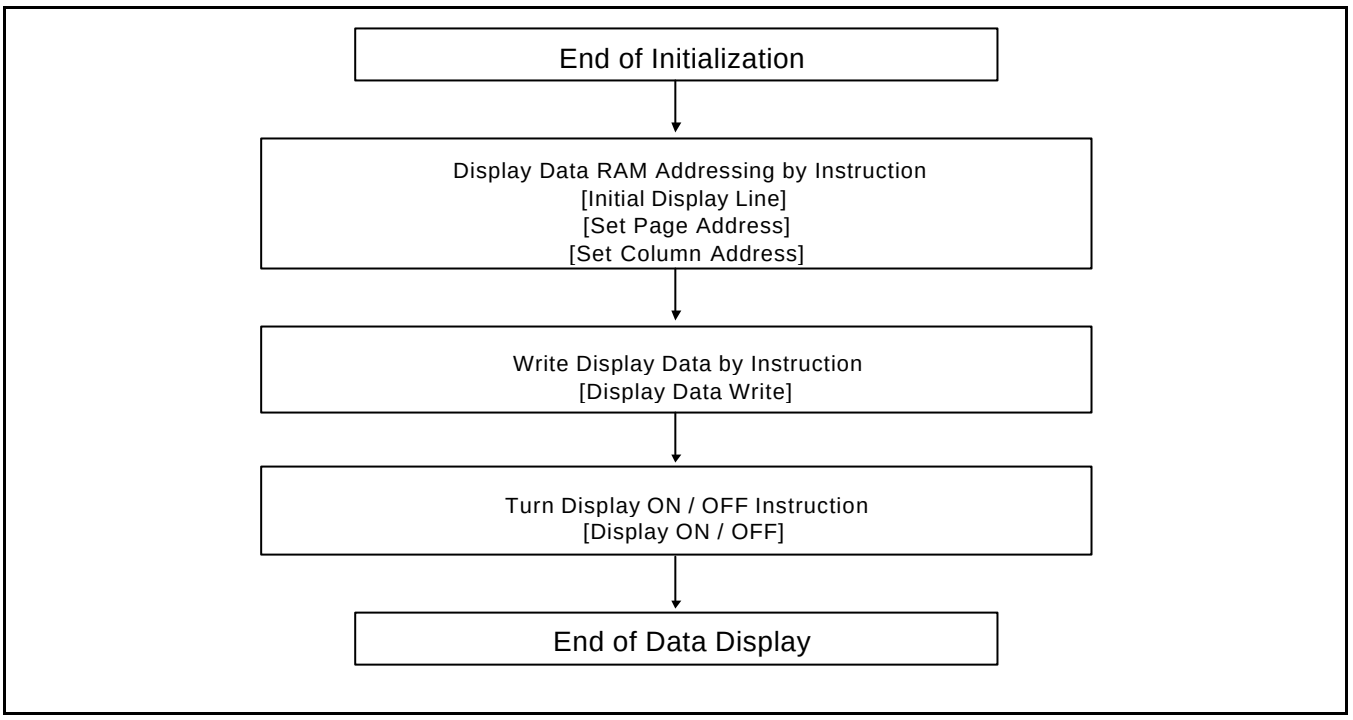


Figure 35. Data Displaying

Referential Instruction Set-up Flow: Power OFF

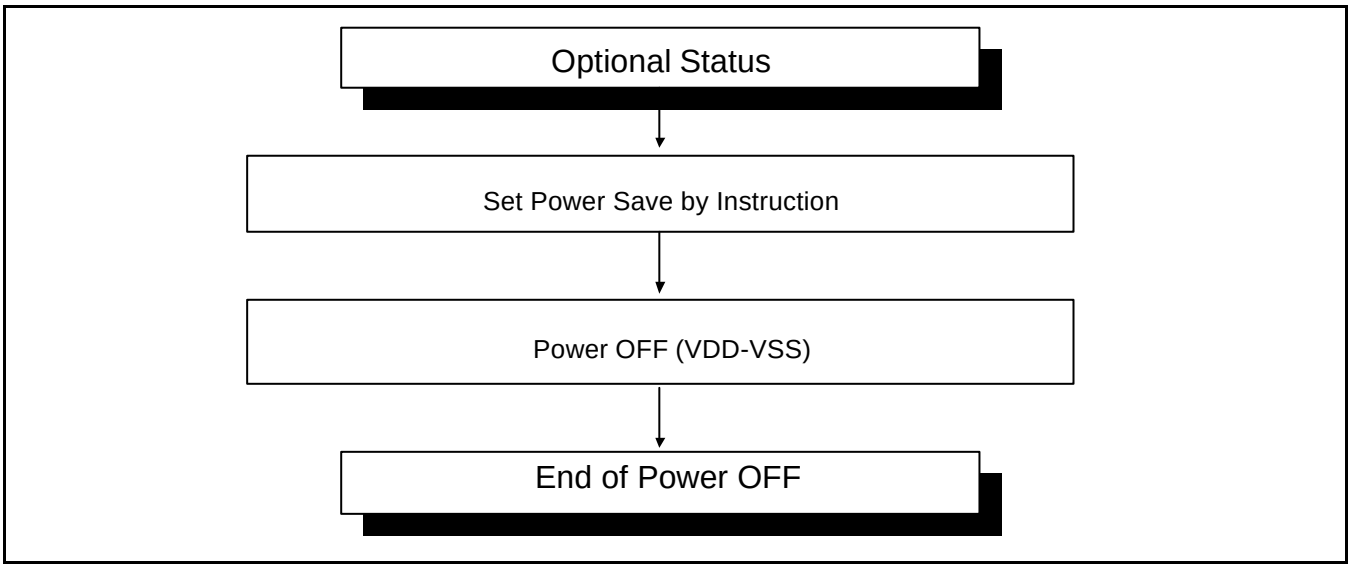


Figure 36. Power OFF

Referential Instruction Set-up Flow: Partial Duty Changing

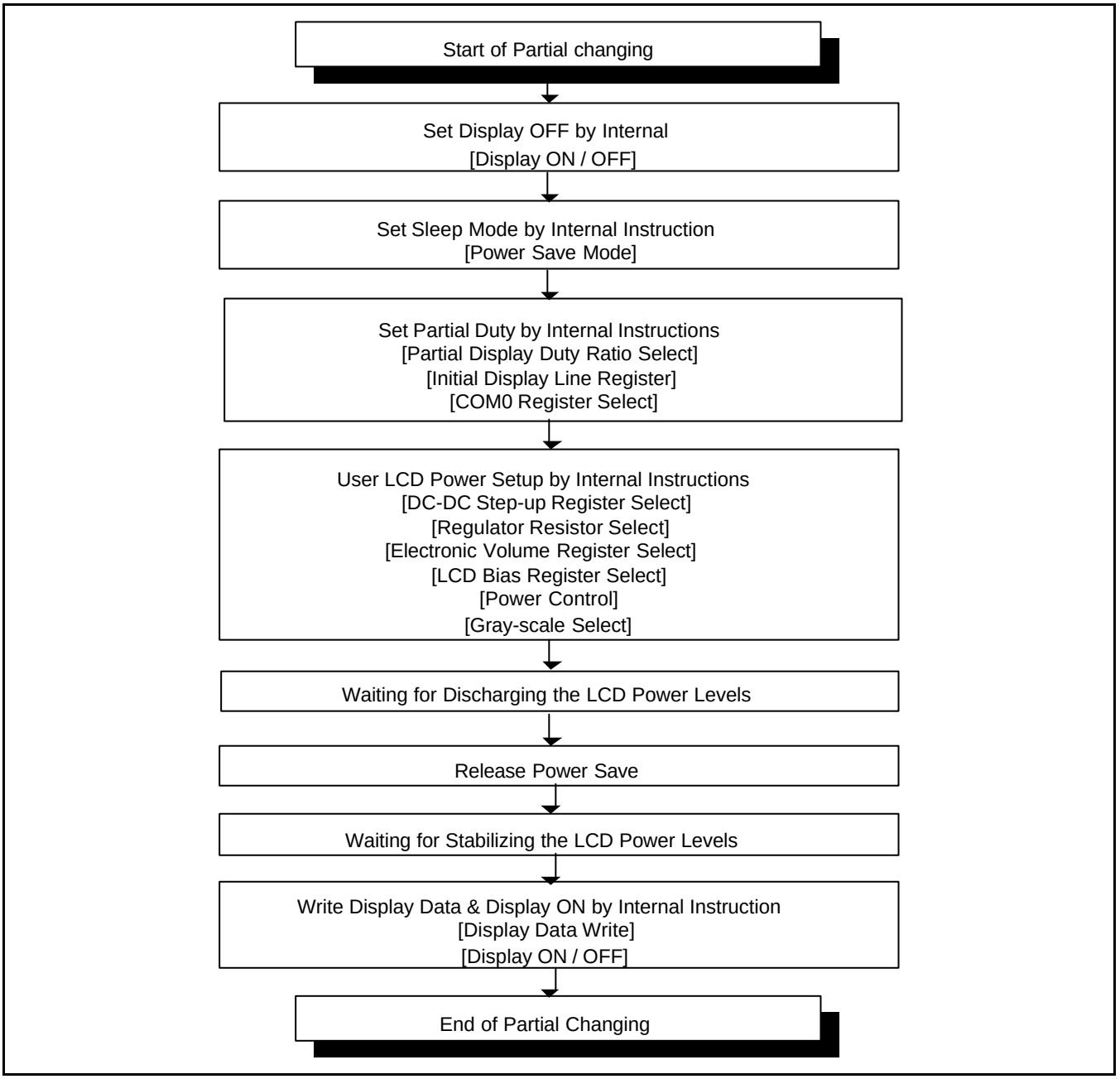


Figure 37. Partial Duty Changing

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 18. Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 ~ + 7.0	V
	V0, VOUT	- 0.3 ~ +17.0	V
	V1, V2, V3, V4	- 0.3 ~ V0 + 0.3	V
External reference voltage	VEXT	+0.3 ~ V_{DD}	
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STR}	- 55 ~ + 125	°C

NOTES:

1. V_{DD}, V0, VOUT, V1 to V4 and VEXT are based on V_{SS} = 0V.
2. Voltages $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ must always be satisfied.(VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 19. DC Characteristics

(V_{SS} = 0V, V_{DD} = 1.8 to 3.3V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		1.8	-	3.3	V	VDD (*1)
Operating voltage (2)		V0		4.0	-	15.0	V	V0 (*2)
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	(*3)
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	(*4)
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	(*3)
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	(*5)
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn (*6)
Operating frequency		f_{FR}	Ta = 25°C 1/128 Duty, 9 PWM REXT = 620kΩ (*11)	70	85	100	Hz	(*7) (*11)
Voltage converter Input voltage		V_{CI}	× 3 / x 4	2.4	-	3.3	V	VCI
			×5	2.4		3.0	V	
Voltage converter output voltage		V_{OUT}	x3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		V_{OUT}		5.4	-	15.0	V	VOUT
Voltage follower operating voltage		V0		4.0	-	11.0	V	V0 (*8)
Reference voltage		V_{REF}	Ta = 25°C	2.04	2.10	2.16	V	(*9)

Dynamic Current Consumption when The Internal Power Supply is ON

Table 20. Dynamic Current 2 (Internal Power)

(V_{DD} = 2.5V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption	I_{DD}	Vci=2.5V, V0 - Vss =9.004V, x5 boosting, duty = 1/81, normal mode (Display Off)	-	60	-	µA	(*10)
		Vci=2.5V, V0 - Vss = 9.004V, x5 boosting, duty = 1/81, normal mode (Display On , Checker Pattern)	-	120	-	µA	(*10)
		Vci=2.5V, V0 - Vss = 10.0V, x5 boosting, duty = 1/81,on LCD module (Display On , Checker Pattern)		400		µA	

Current Consumption during Power Save Mode

Table 21. Power Save Mode Current

(V_{DD} = 2.5V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	During sleep	-	-	2	µA	(*10)

Table 22. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	fCL	Fosc
1/N	On-chip oscillator circuit is used	$f_{FR} \times N$	$f_{FR} \times PWM \times 2 \times N$

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 16 to 129)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CSB, RS, DB0 to DB7, E_RD, RW_WR, RESETB, PS1, PS0, INTRS and REF
*4. DB0 to DB7
*5. Applies when the DB0 to DB7 pins are in high impedance.
*6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
*7. See Table 23 for the relationship between oscillation frequency and frame frequency.
*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON.
The current flowing through voltage regulation resistors(Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.
Other conditions are 1/12 bias, 3 FRC, 9 PWM, Frame inversion, Frame freq. = 85HZ, BL=(9,9,9,0), DG=(6,6,6,0), LG=(3,3,3,0), WH=(0,0,0,0).
*11. Applies when PWM method is used.
When both PWM and FRC method are used, frame frequency should be increased up to more than 130Hz.
So, oscillator resistor value between OSC1 and VDD pin should be reduced.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

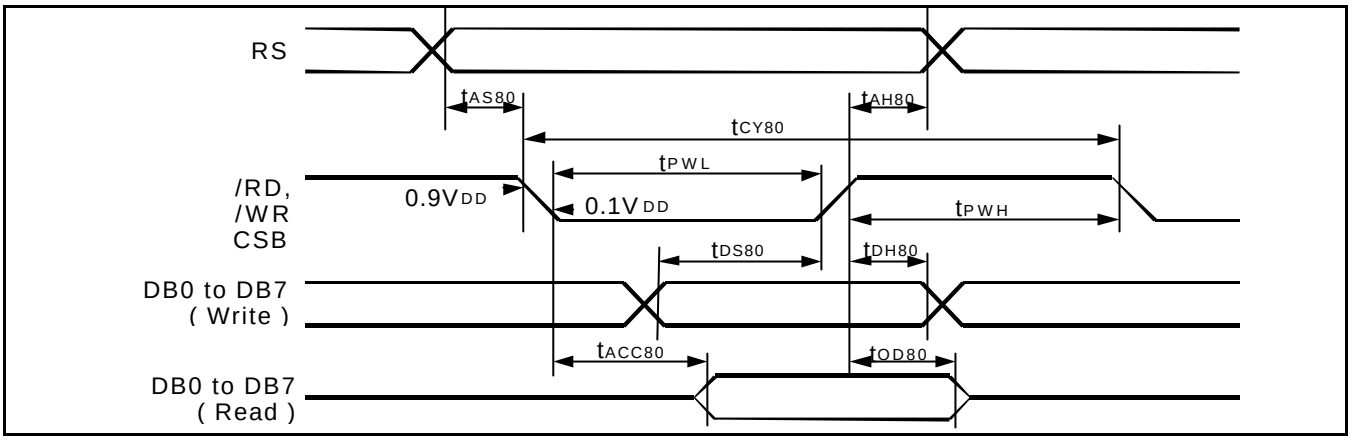


Figure 38. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 1.8V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time for write System cycle time for read		t_{CY80} t_{CY80}		150 330	-	ns
Pulse width low Pulse width high	/WR /RD	t_{PWL} t_{PWH}		60 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		40 10	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	15 10	- 50	ns

(V_{DD} = 2.7V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time for write System cycle time for read		t_{CY80} t_{CY80}		100 166	-	ns
Pulse width low Pulse width high	/WR /RD	t_{PWL} t_{PWH}		40 40	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		30 5	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	15 10	- 50	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, (tr + tf) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read

Read / Write Characteristics (6800-series Microprocessor)

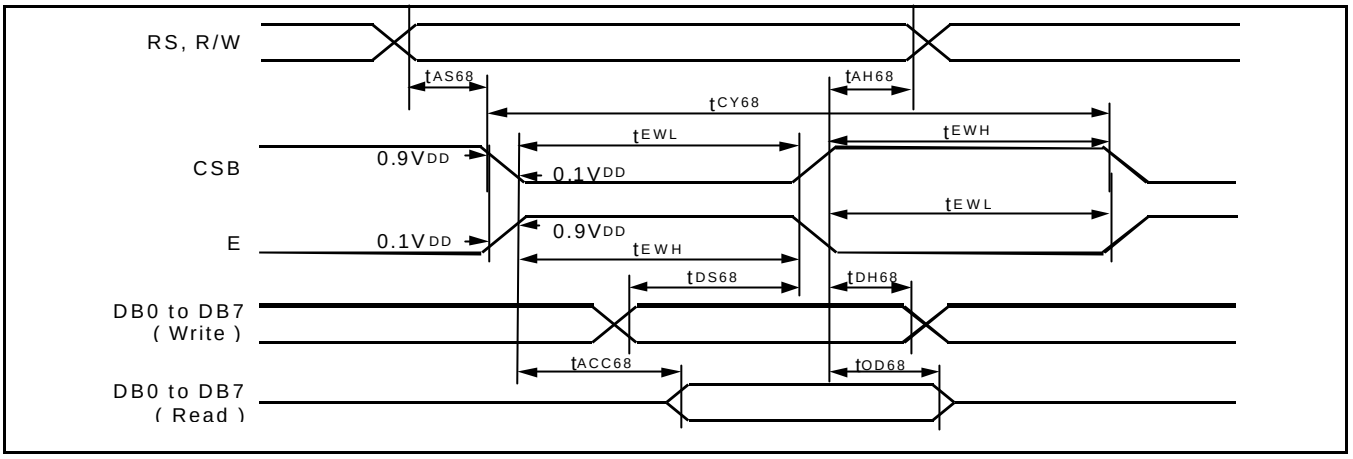


Figure39. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 1.8V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time for write System cycle time for read		t_{CY68} t_{CY68}		150 330	-	ns
Enable width high Enable width low	E_RD (E)	t_{EWH} t_{EWL}		60 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		40 10	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	15 10	- 50	ns

(V_{DD} = 2.7V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time for write System cycle time for read		t_{CY68} t_{CY68}		100 166	-	ns
Enable width high Enable width low	E_RD (E)	t_{EWH} t_{EWL}		40 40	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		30 5	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	15 10	- 50	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (t_{CY68} - t_{EWHW} - t_{EWLW}) for write, (tr + tf) < (t_{CY68} - t_{EWHR} - t_{EWLR}) for read

Serial Interface Characteristics

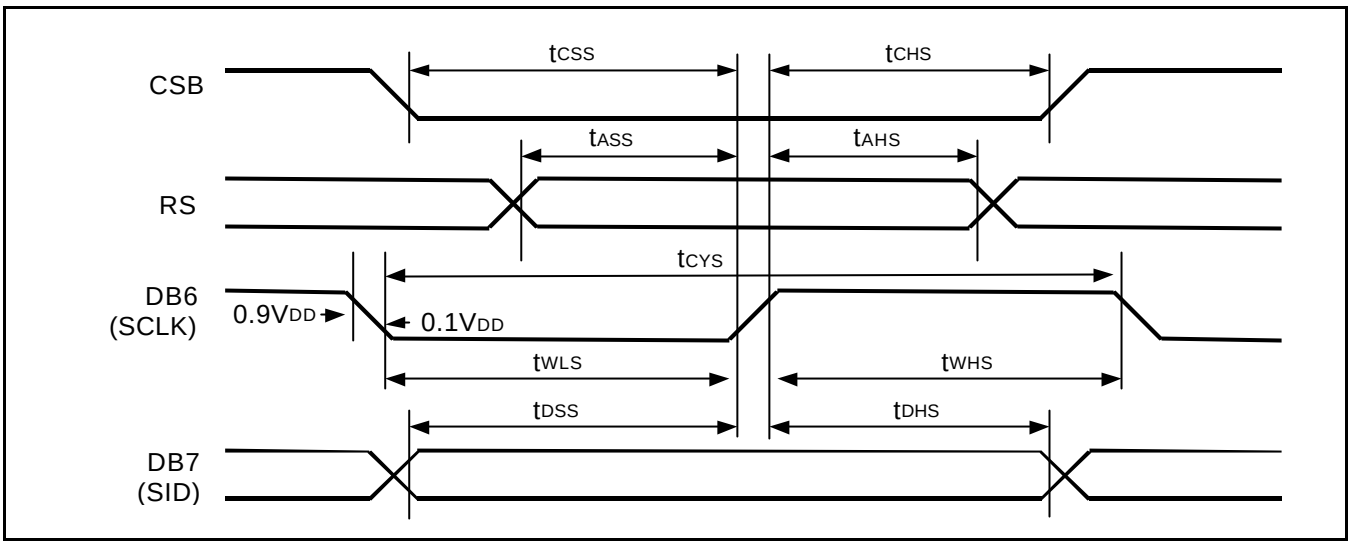


Figure 40. Serial Interface Characteristics

(V_{DD} = 1.8V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		111 60 60	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		60 60	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		60 60	- -	ns
CSB setup time CSB hold time	CSB	t_{CSS} t_{CHS}		60 1/2 * t_{CYS}	- -	ns

(V_{DD} = 2.7V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		58.8 30 30	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		30 30	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		30 30	- -	ns
CSB setup time CSB hold time	CSB	t_{CSS} t_{CHS}		30 1/2 * t_{CYS}	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

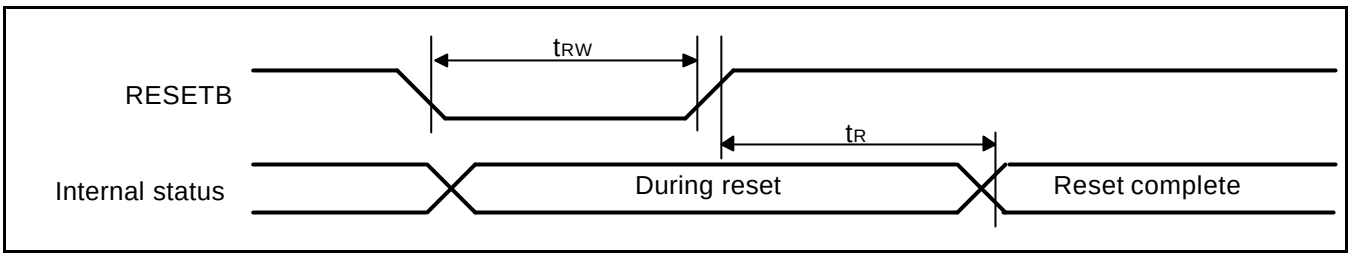


Figure 41. Reset Input Timing

(V_{DD} = 1.8 ~ 3.3V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS0 = “H”, PS1 = “H”)

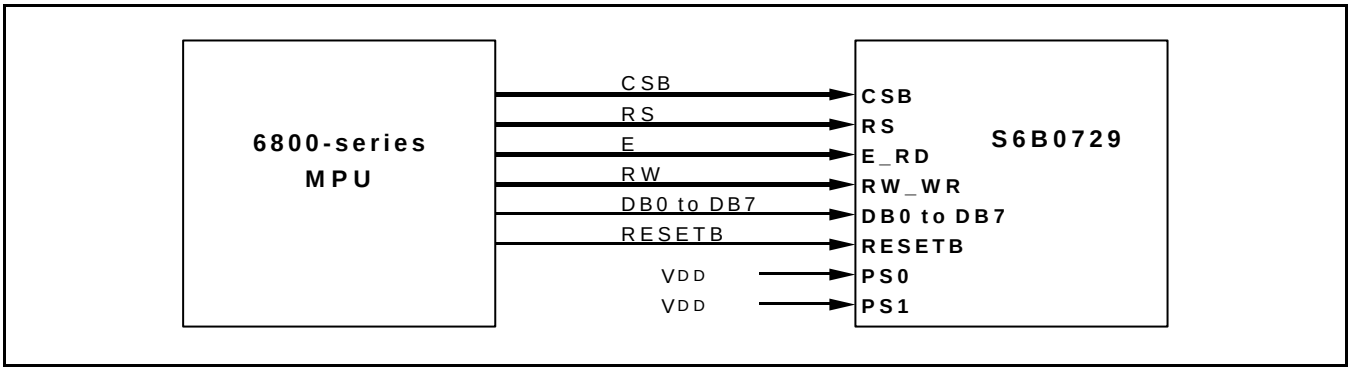


Figure 42. Interfacing with 6800-series (PS0 = “H”, C68 = “H”)

In Case of Interfacing with 8080-series (PS0 = “H”, PS1 = “L”)

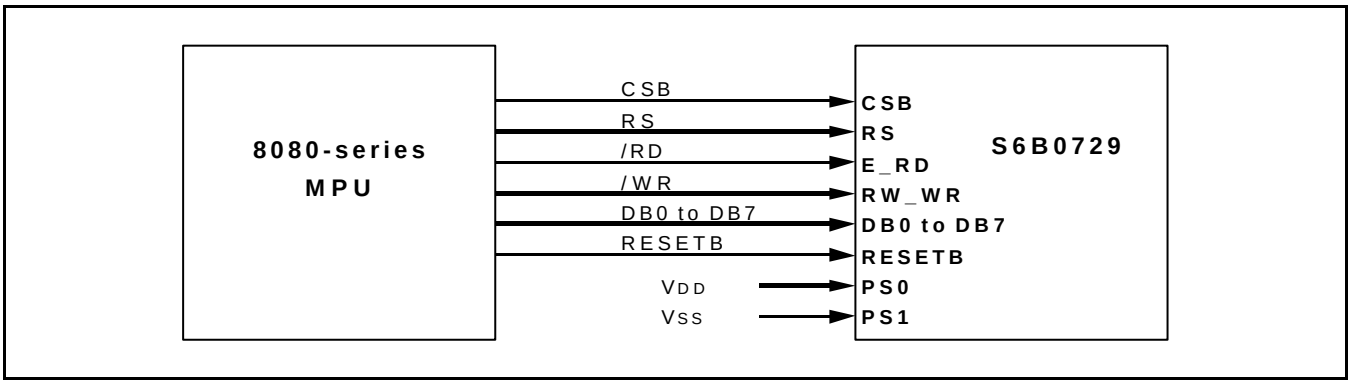


Figure 43. Interfacing with 8080-series (PS0 = “H”, C68 = “L”)

In Case of 4-pin SPI mode (PS0 = "L" , PS1 = "H")

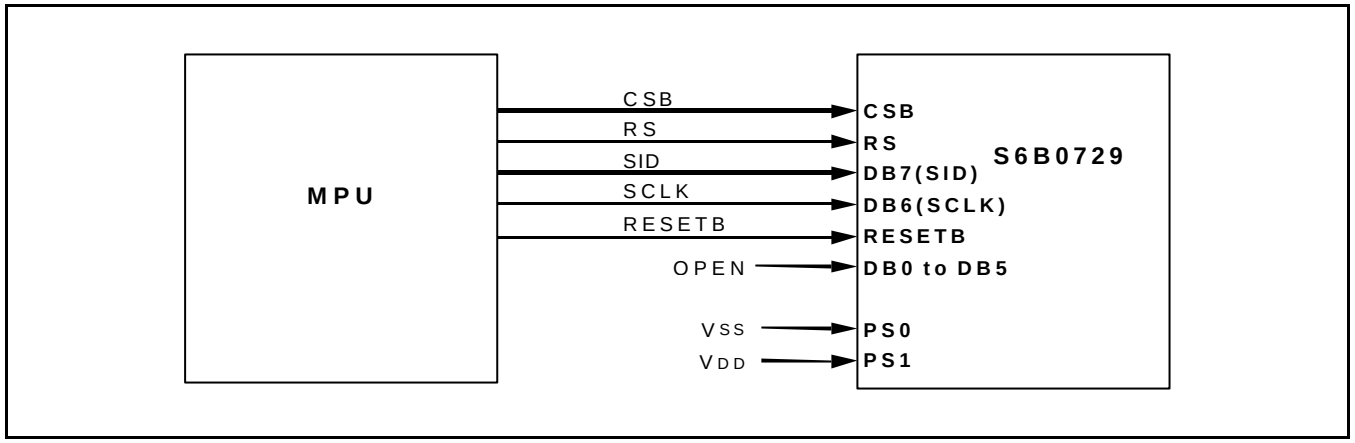


Figure 44. Serial Interface (PS0 = “L”, PS1 = “H”)

In Case of 3-pin SPI mode (PS0 = "L" , PS1 = "L")

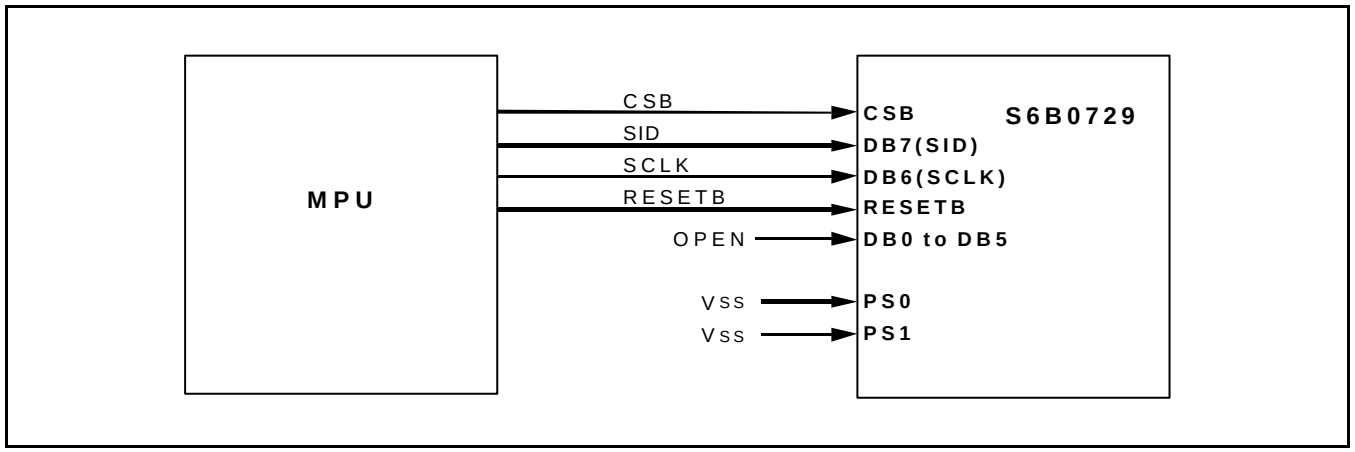


Figure 45. Serial Interface (PS0 = “L”, PS1 = “L”)

CONNECTIONS BETWEEN S6B0729 AND LCD PANEL

Single Chip Configuration (1/81 Duty Configurations)

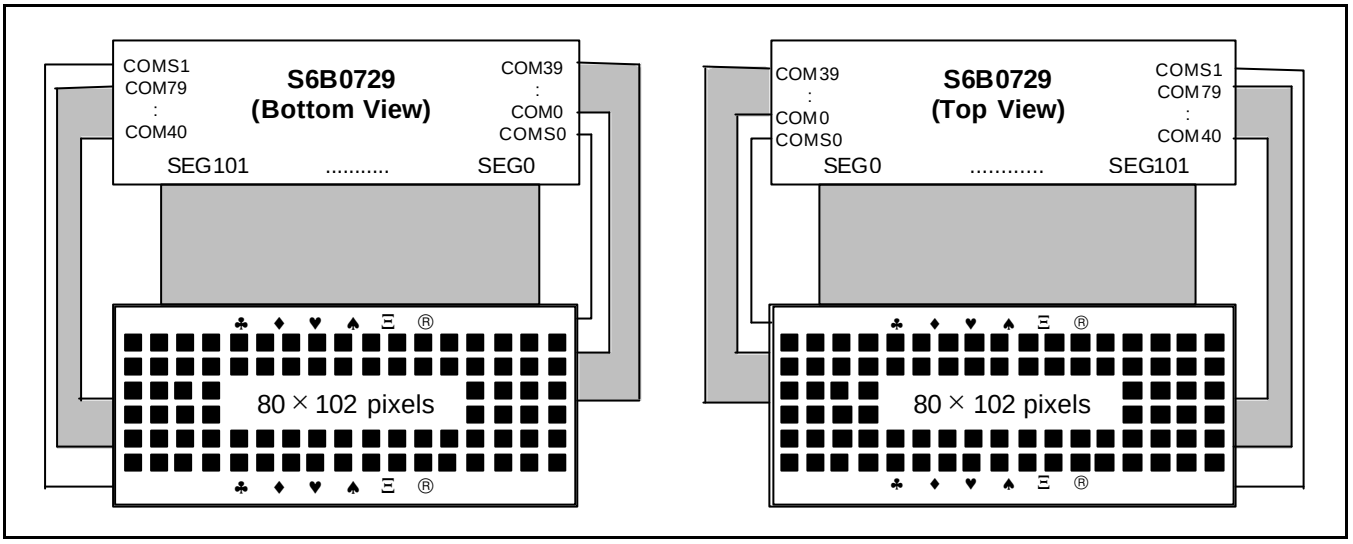


Figure 46. SHL = 0, ADC = 1

Figure 47. SHL = 0, ADC = 0

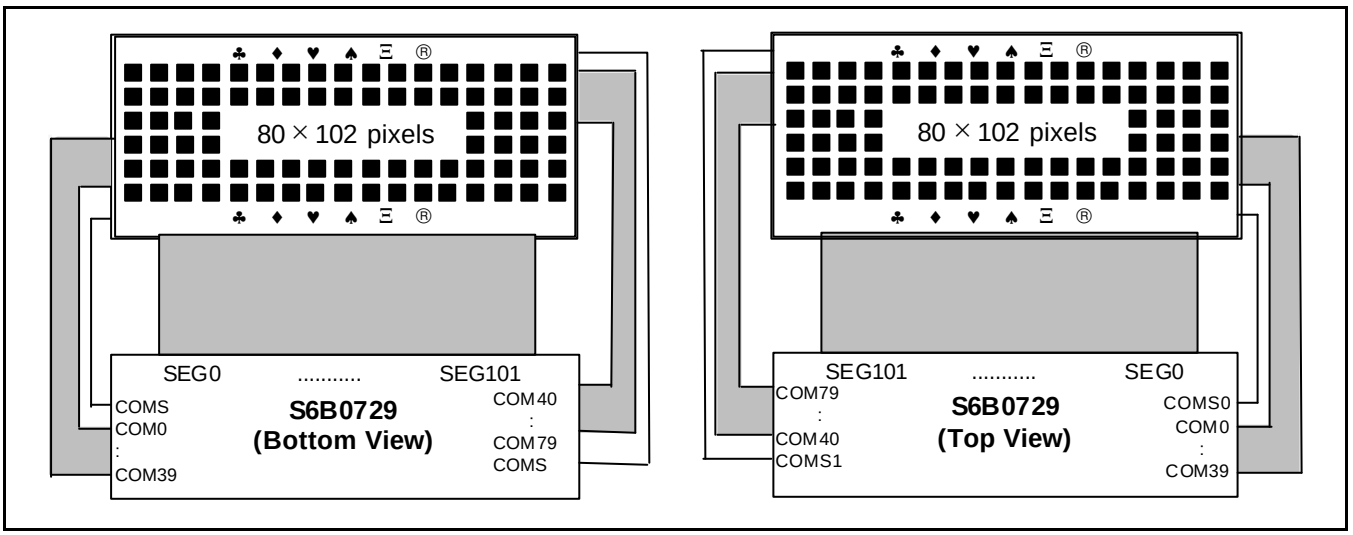


Figure 48. SHL = 1, ADC = 0

Figure 49. SHL = 1, ADC = 1